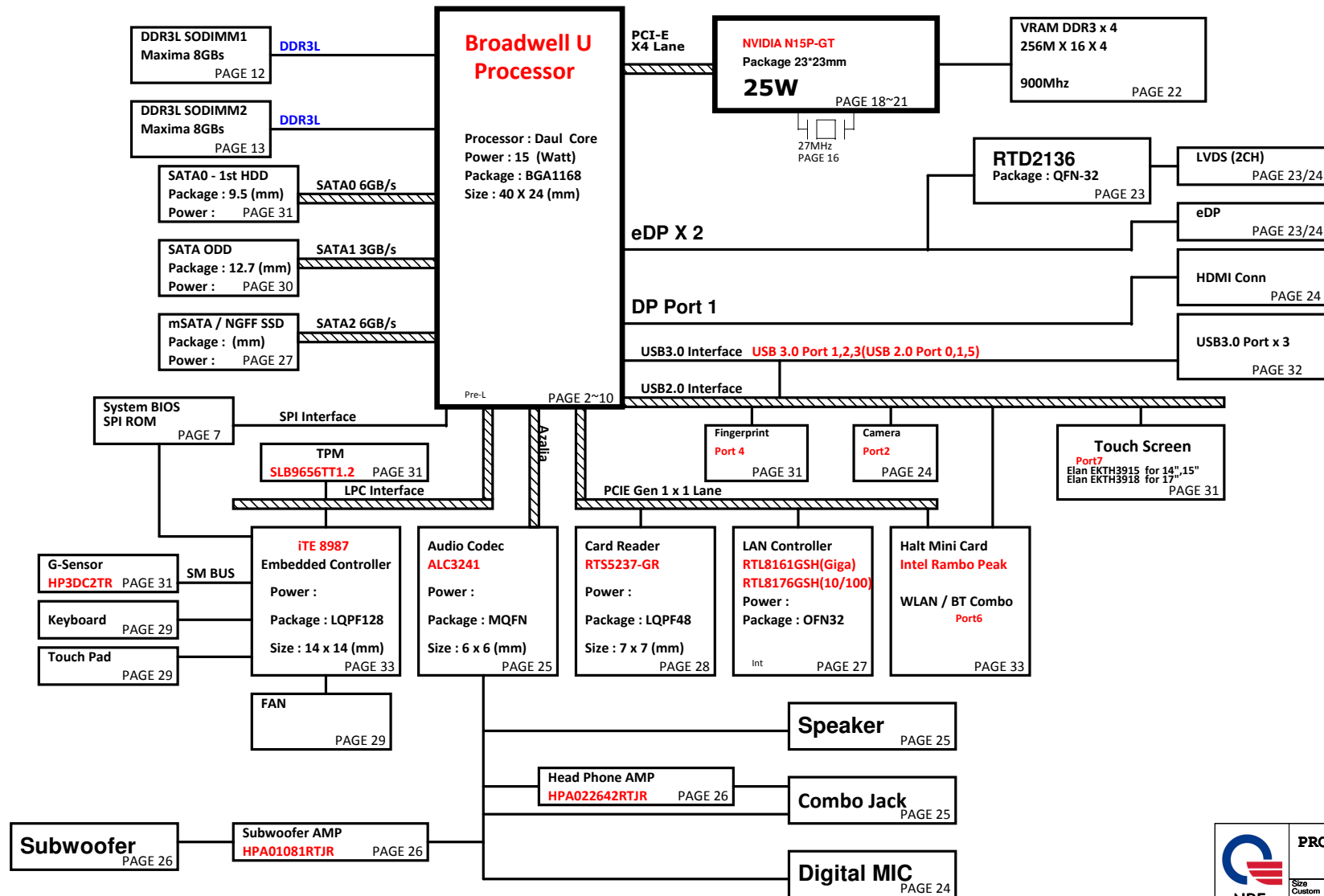



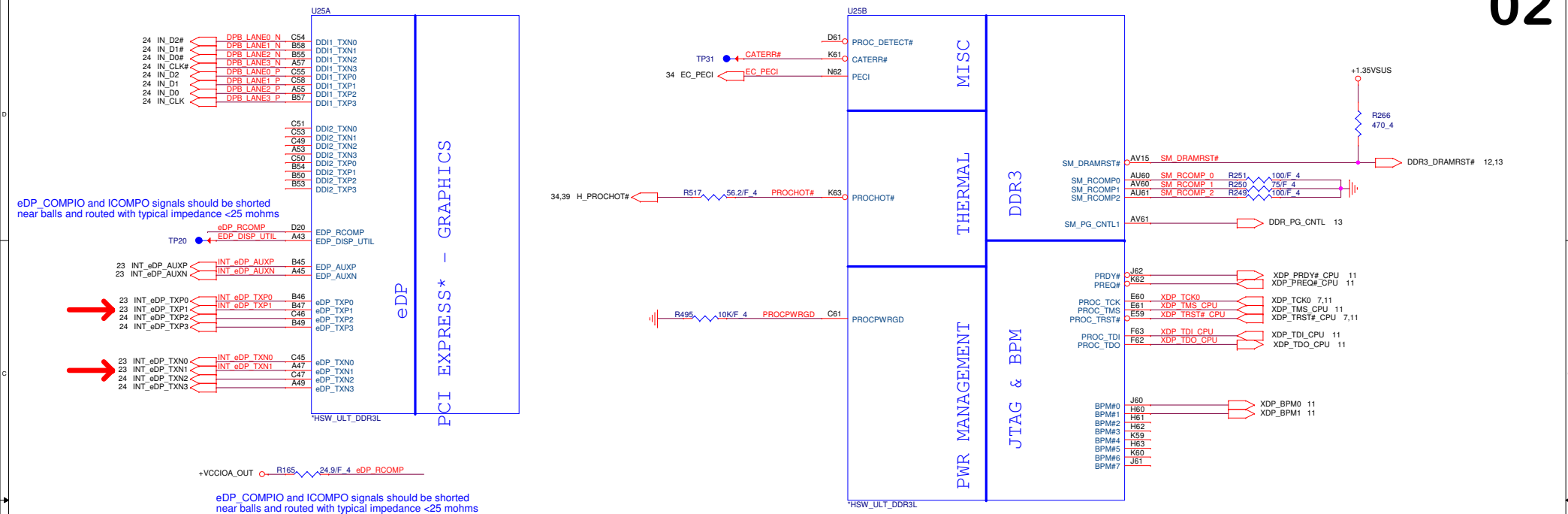
DIS (14" / 15" / 17") Lay-Vine Intel Crescent Bay ULT Platform Block Diagram

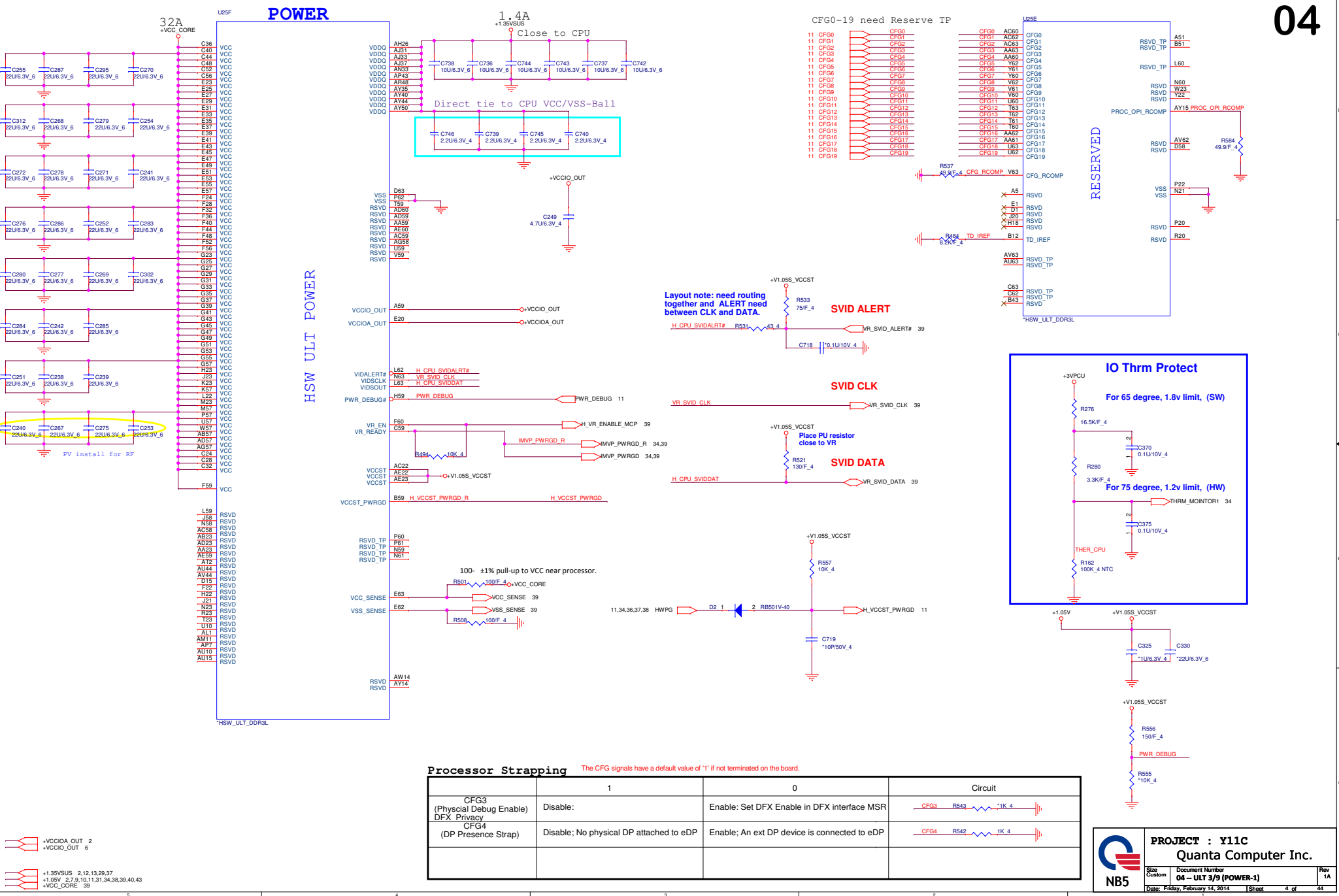
PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT



		PROJECT : Y11C	
		Quanta Computer Inc.	
Size Custom	Document Number Block Diagram	Date: Friday, February 14, 2014	Sheet 1 of 44
NB5			Rev 1A

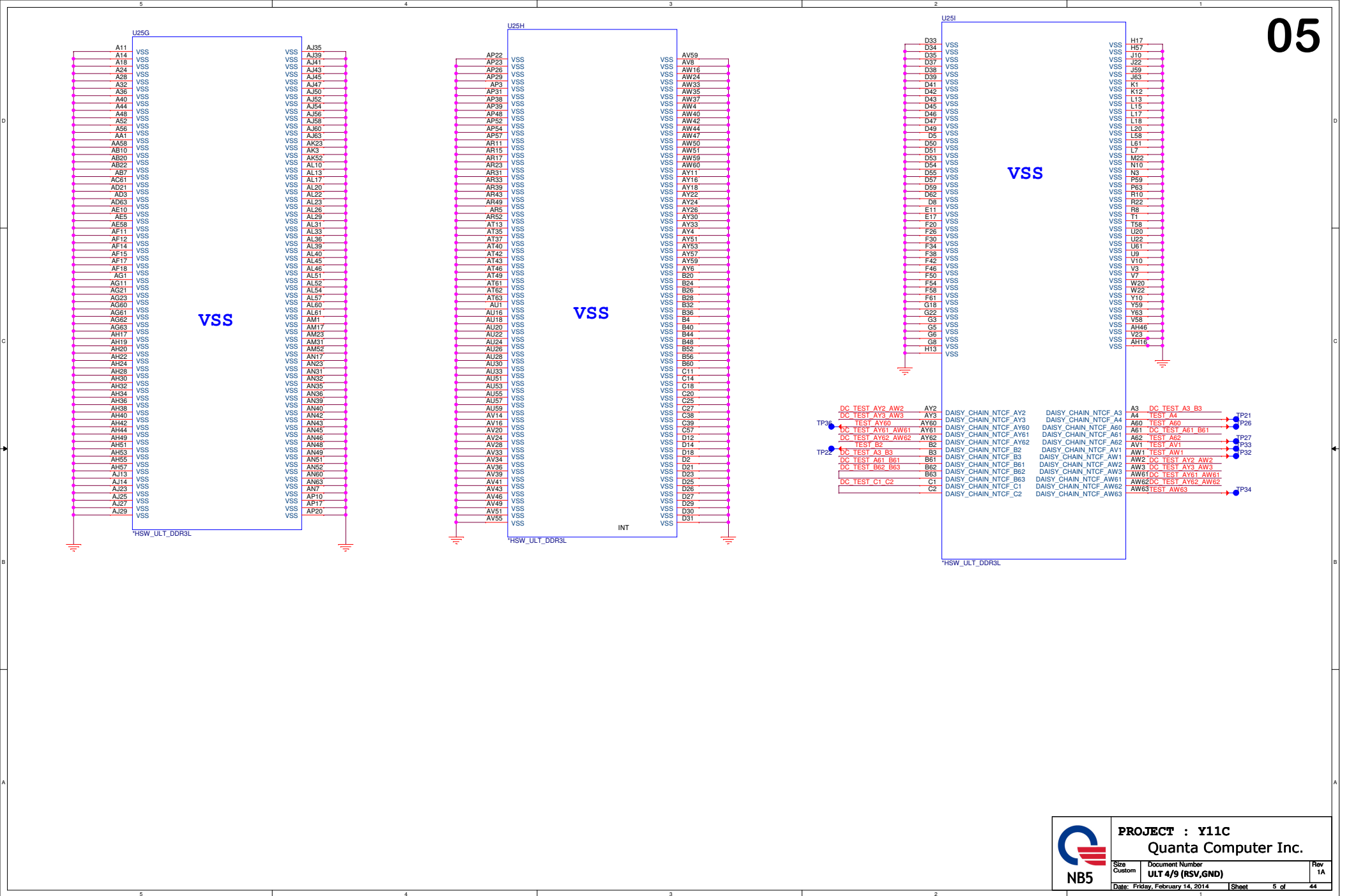


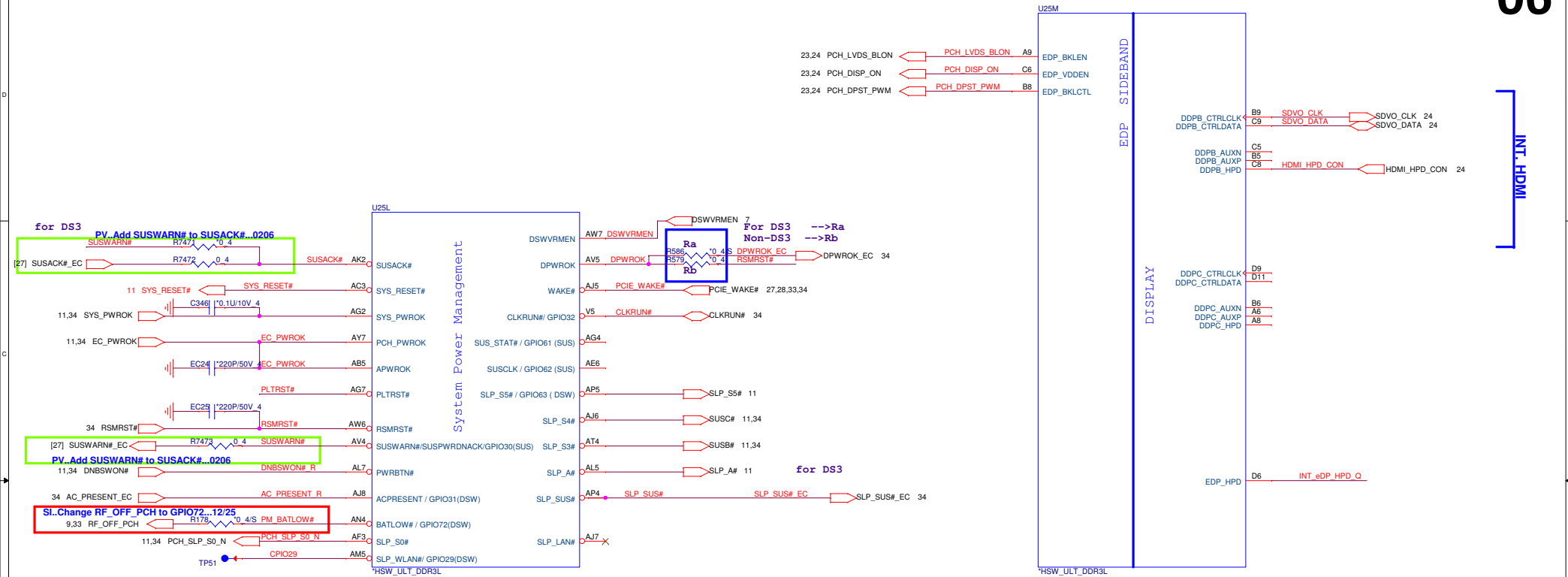


PROJECT : Y11C
Quanta Computer Inc.

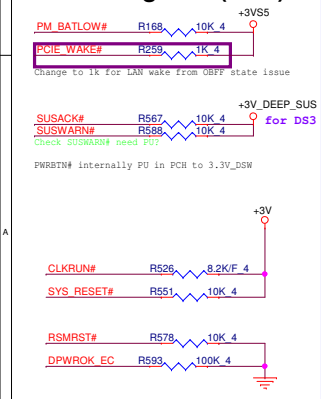
Size Custom	Document Number 04 - ULT 3/9 (POWER-1)	Rev 1A
Date: Friday, February 14, 2014		Sheet 4 of 44

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 RS43 1K 4
CFG4 (DP Presence Strap)	Disable: No physical DP attached to eDP	Enable: An ext DP device is connected to eDP	CFG4 RS42 1K 4

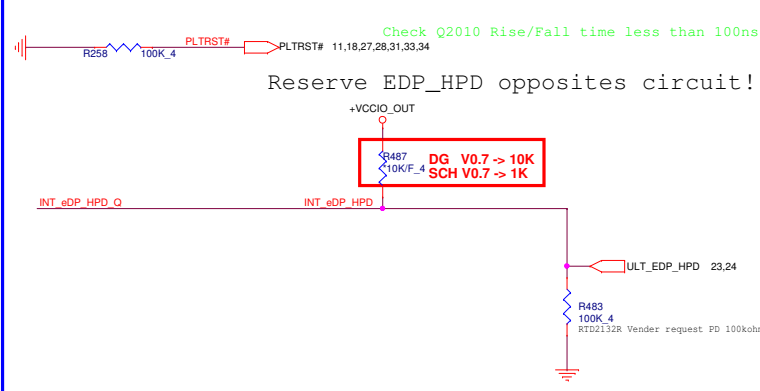




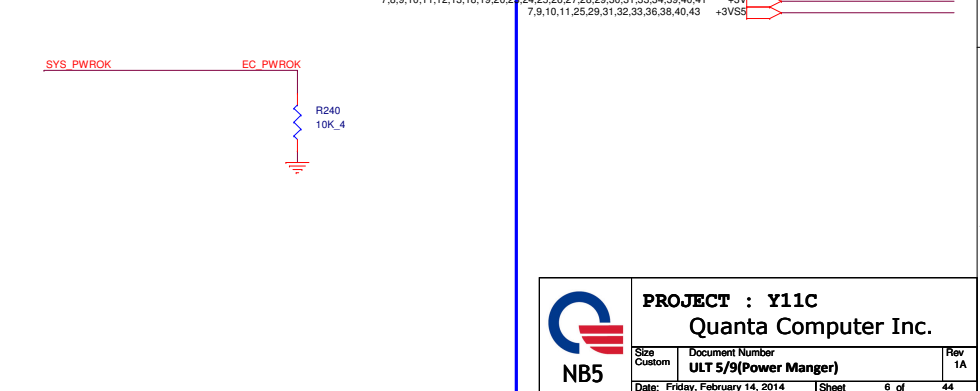
PCH Pull-high/low(CLG)






PLTRST#(CLG)



System PWR_OK(CLG)



[illegible]

Pin Name	Strap description	Sampled	Configuration	Circuit						
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode							
SDIO_D0 /GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)							
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC 						
HDA_SDO /I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overriden	34 GPIO33_EC 						
GPIO_MOSI /GPIO86	Boot BIOS Selection	PWROK	<table border="1" data-bbox="676 1055 856 1096"> <tr> <th>GNT0#</th><th>Boot Location</th></tr> <tr> <td>1</td><td>LPC</td></tr> <tr> <td>0</td><td>SPI(Default)</td></tr> </table>	GNT0#	Boot Location	1	LPC	0	SPI(Default)	
GNT0#	Boot Location									
1	LPC									
0	SPI(Default)									
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality							
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up	+3V_RTC 						
				<div data-bbox="1062 1284 1337 1334"> <div>34 PCH_SPI_CS0#_R</div> <div>34 PCH_SPI1_CLK_R</div> <div>34 PCH_SPI1_SI_R</div> <div>34 PCH_SPI1_SO_R</div> <div> <div>PCH_SPI_CS0#_R</div> <div>PCH_SPI1_CLK_R</div> <div>PCH_SPI1_SI_R</div> <div>PCH_SPI1_SO_R</div> </div> </div>						

no stuff If use green Clock

[illegible]

The schematic diagram illustrates the electrical connections between the ACZ_001 module and the ACZ_000 module. Key components and connections include:

- Resistors:** R574 (1K 4), R585 (33 4), R590 (33 4), R589 (33 4), and R591 (33 4) are used for signal conditioning.
- Capacitor:** C741 (10P/50V_4) is connected to the ground for the BIT_CLK_AUDIO signal.
- Signal Connections:**
 - ACZ_SYNC:** Connected to R574 and ACZ_SYNC.
 - ACZ_SYNC_AUDIO:** Connected to R585 and ACZ_SYNC.
 - ACZ_RST#:** Connected to R590 and ACZ_RST#.
 - ACZ_SDOUT:** Connected to R589 and ACZ_SDOUT.
 - BIT_CLK_AUDIO:** Connected to R591 and BIT_CLK_AUDIO.
- Table of Connections:**

Signal	Component	Value	Destination
ACC_LED#	R538	10K 4	ACC_LED#
SIO_EXT_SMI#	R528	10K 4	SIO_EXT_SMI#
PCI_SERP#	R527	10K 4	PCI_SERP#
SATA3gP	R550	10K 4	SATA3gP

U10&U15 footprint 要重疊

PCH SPI ROM(CLG)

TP24, TP23, TP20, TP21, TP22, TP20 need place to TOP

R457/R453/R450/R451/R546/R548 close to U15 pin

Pin connections and component values:

- Pin 1: PCH SPI CS0# R
- Pin 2: PCH SPI CLK R
- Pin 3: PCH SPI SI R
- Pin 4: PCH SPI SO R
- Pin 5: BIOS WP#
- Pin 6: PCH SPI CS0# R
- Pin 7: PCH SPI CLK R
- Pin 8: PCH SPI SI R
- Pin 9: PCH SPI SO R
- Pin 10: BIOS WP#
- Pin 11: HOLD#
- Pin 12: PCH SPI CS0# R
- Pin 13: PCH SPI CLK R
- Pin 14: PCH SPI SI R
- Pin 15: PCH SPI SO R
- Pin 16: BIOS WP#
- Pin 17: HOLD#
- Pin 18: PCH SPI CS0# R
- Pin 19: PCH SPI CLK R
- Pin 20: PCH SPI SI R
- Pin 21: PCH SPI SO R
- Pin 22: BIOS WP#
- Pin 23: HOLD#
- Pin 24: PCH SPI CS0# R
- Pin 25: PCH SPI CLK R
- Pin 26: PCH SPI SI R
- Pin 27: PCH SPI SO R
- Pin 28: BIOS WP#
- Pin 29: HOLD#
- Pin 30: PCH SPI CS0# R
- Pin 31: PCH SPI CLK R
- Pin 32: PCH SPI SI R
- Pin 33: PCH SPI SO R
- Pin 34: BIOS WP#
- Pin 35: HOLD#
- Pin 36: PCH SPI CS0# R
- Pin 37: PCH SPI CLK R
- Pin 38: PCH SPI SI R
- Pin 39: PCH SPI SO R
- Pin 40: BIOS WP#
- Pin 41: HOLD#
- Pin 42: PCH SPI CS0# R
- Pin 43: PCH SPI CLK R
- Pin 44: PCH SPI SI R
- Pin 45: PCH SPI SO R
- Pin 46: BIOS WP#
- Pin 47: HOLD#
- Pin 48: PCH SPI CS0# R
- Pin 49: PCH SPI CLK R
- Pin 50: PCH SPI SI R
- Pin 51: PCH SPI SO R
- Pin 52: BIOS WP#
- Pin 53: HOLD#
- Pin 54: PCH SPI CS0# R
- Pin 55: PCH SPI CLK R
- Pin 56: PCH SPI SI R
- Pin 57: PCH SPI SO R
- Pin 58: BIOS WP#
- Pin 59: HOLD#
- Pin 60: PCH SPI CS0# R
- Pin 61: PCH SPI CLK R
- Pin 62: PCH SPI SI R
- Pin 63: PCH SPI SO R
- Pin 64: BIOS WP#
- Pin 65: HOLD#
- Pin 66: PCH SPI CS0# R
- Pin 67: PCH SPI CLK R
- Pin 68: PCH SPI SI R
- Pin 69: PCH SPI SO R
- Pin 70: BIOS WP#
- Pin 71: HOLD#
- Pin 72: PCH SPI CS0# R
- Pin 73: PCH SPI CLK R
- Pin 74: PCH SPI SI R
- Pin 75: PCH SPI SO R
- Pin 76: BIOS WP#
- Pin 77: HOLD#
- Pin 78: PCH SPI CS0# R
- Pin 79: PCH SPI CLK R
- Pin 80: PCH SPI SI R
- Pin 81: PCH SPI SO R
- Pin 82: BIOS WP#
- Pin 83: HOLD#
- Pin 84: PCH SPI CS0# R
- Pin 85: PCH SPI CLK R
- Pin 86: PCH SPI SI R
- Pin 87: PCH SPI SO R
- Pin 88: BIOS WP#
- Pin 89: HOLD#
- Pin 90: PCH SPI CS0# R
- Pin 91: PCH SPI CLK R
- Pin 92: PCH SPI SI R
- Pin 93: PCH SPI SO R
- Pin 94: BIOS WP#
- Pin 95: HOLD#
- Pin 96: PCH SPI CS0# R
- Pin 97: PCH SPI CLK R
- Pin 98: PCH SPI SI R
- Pin 99: PCH SPI SO R
- Pin 100: BIOS WP#
- Pin 101: HOLD#
- Pin 102: PCH SPI CS0# R
- Pin 103: PCH SPI CLK R
- Pin 104: PCH SPI SI R
- Pin 105: PCH SPI SO R
- Pin 106: BIOS WP#
- Pin 107: HOLD#
- Pin 108: PCH SPI CS0# R
- Pin 109: PCH SPI CLK R
- Pin 110: PCH SPI SI R
- Pin 111: PCH SPI SO R
- Pin 112: BIOS WP#
- Pin 113: HOLD#
- Pin 114: PCH SPI CS0# R
- Pin 115: PCH SPI CLK R
- Pin 116: PCH SPI SI R
- Pin 117: PCH SPI SO R
- Pin 118: BIOS WP#
- Pin 119: HOLD#
- Pin 120: PCH SPI CS0# R
- Pin 121: PCH SPI CLK R
- Pin 122: PCH SPI SI R
- Pin 123: PCH SPI SO R
- Pin 124: BIOS WP#
- Pin 125: HOLD#
- Pin 126: PCH SPI CS0# R
- Pin 127: PCH SPI CLK R
- Pin 128: PCH SPI SI R
- Pin 129: PCH SPI SO R
- Pin 130: BIOS WP#
- Pin 131: HOLD#
- Pin 132: PCH SPI CS0# R
- Pin 133: PCH SPI CLK R
- Pin 134: PCH SPI SI R
- Pin 135: PCH SPI SO R
- Pin 136: BIOS WP#
- Pin 137: HOLD#
- Pin 138: PCH SPI CS0# R
- Pin 139: PCH SPI CLK R
- Pin 140: PCH SPI SI R
- Pin 141: PCH SPI SO R
- Pin 142: BIOS WP#
- Pin 143: HOLD#
- Pin 144: PCH SPI CS0# R
- Pin 145: PCH SPI CLK R
- Pin 146: PCH SPI SI R
- Pin 147: PCH SPI SO R
- Pin 148: BIOS WP#
- Pin 149: HOLD#
- Pin 150: PCH SPI CS0# R
- Pin 151: PCH SPI CLK R
- Pin 152: PCH SPI SI R
- Pin 153: PCH SPI SO R
- Pin 154: BIOS WP#
- Pin 155: HOLD#
- Pin 156: PCH SPI CS0# R
- Pin 157: PCH SPI CLK R
- Pin 158: PCH SPI SI R
- Pin 159: PCH SPI SO R
- Pin 160: BIOS WP#
- Pin 161: HOLD#
- Pin 162: PCH SPI CS0# R
- Pin 163: PCH SPI CLK R
- Pin 164: PCH SPI SI R
- Pin 165: PCH SPI SO R
- Pin 166: BIOS WP#
- Pin 167: HOLD#
- Pin 168: PCH SPI CS0# R
- Pin 169: PCH SPI CLK R
- Pin 170: PCH SPI SI R
- Pin 171: PCH SPI SO R
- Pin 172: BIOS WP#
- Pin 173: HOLD#
- Pin 174: PCH SPI CS0# R
- Pin 175: PCH SPI CLK R
- Pin 176: PCH SPI SI R
- Pin 177: PCH SPI SO R
- Pin 178: BIOS WP#
- Pin 179: HOLD#
- Pin 180: PCH SPI CS0# R
- Pin 181: PCH SPI CLK R
- Pin 182: PCH SPI SI R
- Pin 183: PCH SPI SO R
- Pin 184: BIOS WP#
- Pin 185: HOLD#
- Pin 186: PCH SPI CS0# R
- Pin 187: PCH SPI CLK R
- Pin 188: PCH SPI SI R
- Pin 189: PCH SPI SO R
- Pin 190: BIOS WP#
- Pin 191: HOLD#
- Pin 192: PCH SPI CS0# R
- Pin 193: PCH SPI CLK R
- Pin 194: PCH SPI SI R
- Pin 195: PCH SPI SO R
- Pin 196: BIOS WP#
- Pin 197: HOLD#
- Pin 198: PCH SPI CS0# R
- Pin 199: PCH SPI CLK R
- Pin 200: PCH SPI SI R
- Pin 201: PCH SPI SO R
- Pin 202: BIOS WP#
- Pin 203: HOLD#
- Pin 204: PCH SPI CS0# R
- Pin 205: PCH SPI CLK R
- Pin 206: PCH SPI SI R
- Pin 207: PCH SPI SO R
- Pin 208: BIOS WP#
- Pin 209: HOLD#
- Pin 210: PCH SPI CS0# R
- Pin 211: PCH SPI CLK R
- Pin 212: PCH SPI SI R
- Pin 213: PCH SPI SO R
- Pin 214: BIOS WP#
- Pin 215: HOLD#
- Pin 216: PCH SPI CS0# R
- Pin 217: PCH SPI CLK R
- Pin 218: PCH SPI SI R
- Pin 219: PCH SPI SO R
- Pin 220: BIOS WP#
- Pin 221: HOLD#
- Pin 222: PCH SPI CS0# R
- Pin 223: PCH SPI CLK R
- Pin 224: PCH SPI SI R
- Pin 225: PCH SPI SO R
- Pin 226: BIOS WP#
- Pin 227: HOLD#
- Pin 228: PCH SPI CS0# R
- Pin 229: PCH SPI CLK R
- Pin 230: PCH SPI SI R
- Pin 231: PCH SPI SO R
- Pin 232: BIOS WP#
- Pin 233: HOLD#
- Pin 234: PCH SPI CS0# R
- Pin 235: PCH SPI CLK R
- Pin 236: PCH SPI SI R
- Pin 237: PCH SPI SO R
- Pin 238: BIOS WP#
- Pin 239: HOLD#
- Pin 240: PCH SPI CS0# R
- Pin 241: PCH SPI CLK R
- Pin 242: PCH SPI SI R
- Pin 243: PCH SPI SO R
- Pin

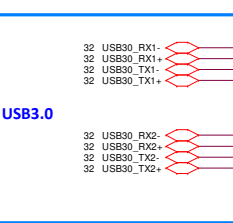
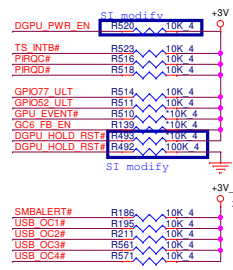
PROJECT : YL12
Quantum Computer Inc.

Size	Document Number	Rev
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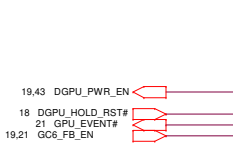
Date: Friday, 12/11/2014 Sheet 7 of 44

Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA)

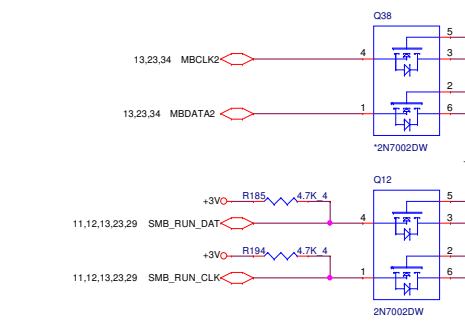
PCI/USB0# Pull-up(CLG)



20111130 Modify USB3.0 for HM70



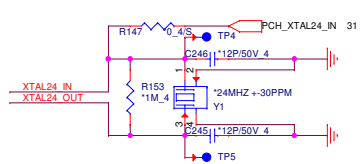
SMBus/Pull-up(CLG)



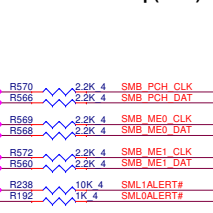
CLK_REQ/Strap Pin(CLG)




CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)

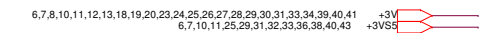
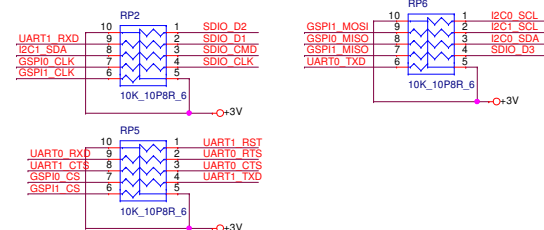





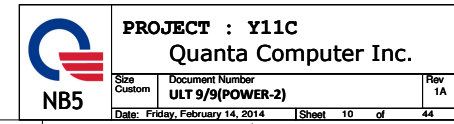
PROJECT : Y11C
Quanta Computer Inc.
Size Custom
Document Number **ULT 7/9 (PCIe/USB/CLK)**
Date: Friday, February 14, 2014
Rev 1A
8 of 44

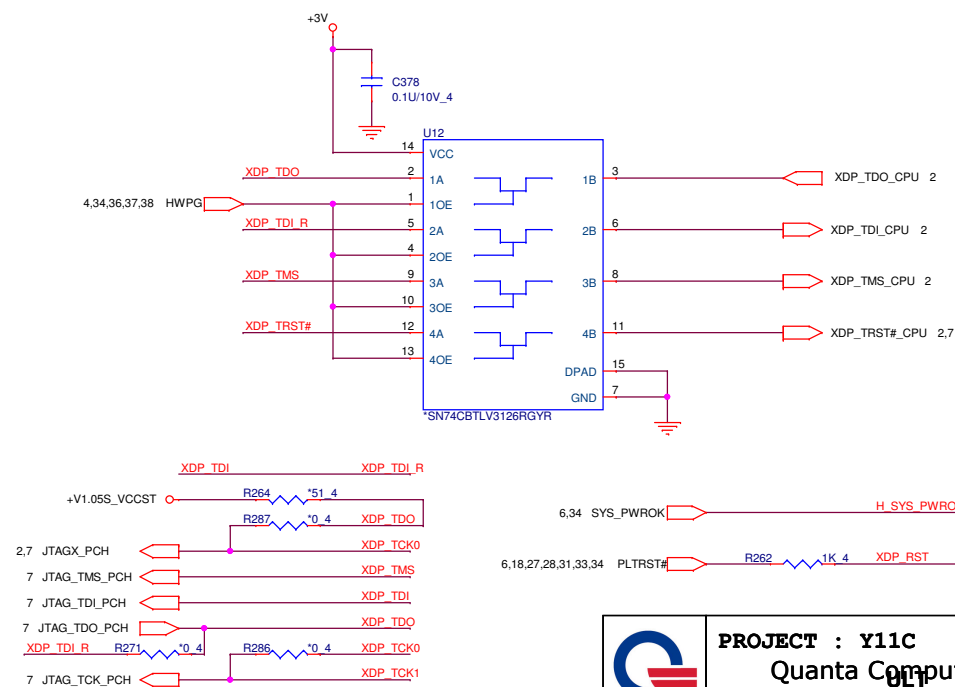
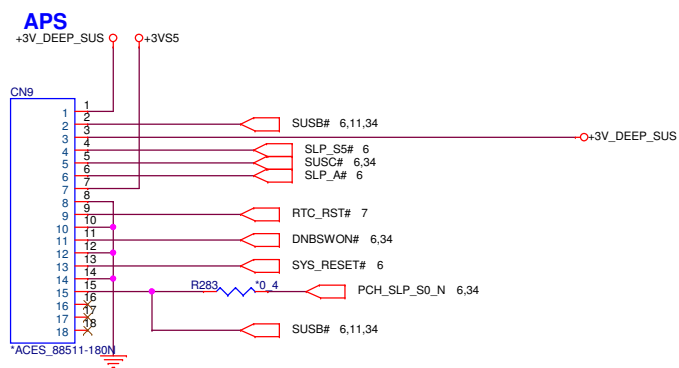
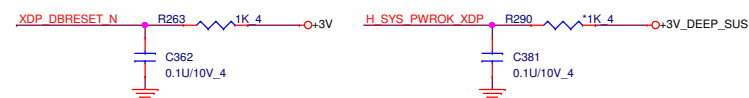
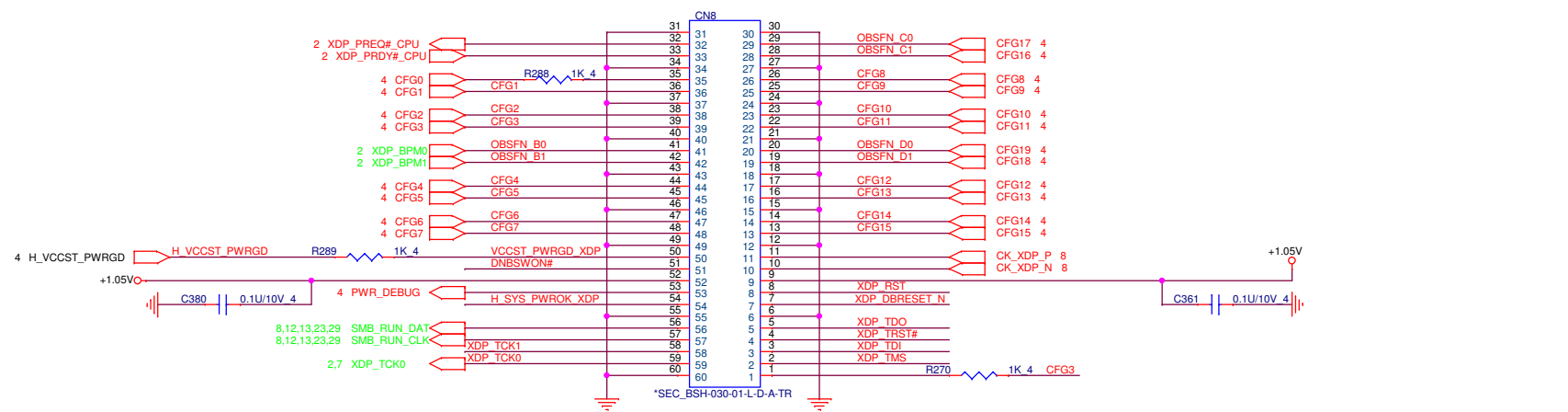
6,7,9,10,11,12,13,18,19,20,23,24,25,26,27,28,29,30,31,33,34,39,40,41
+3V
+3V_DEEP_SUS

09

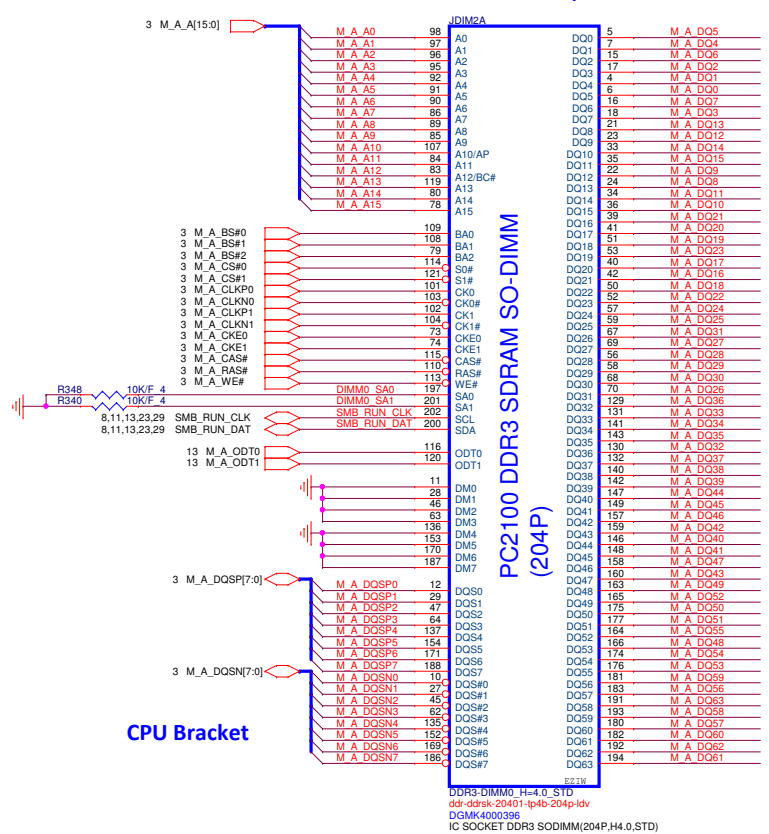


	PROJECT : Y11C Quanta Computer Inc.		
	Size Custom	Document Number ULT 8/9 (GPIO/MISC)	Rev 1A
NB5	Date: Friday, February 14, 2014	Sheet 9 of	44

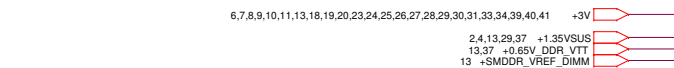
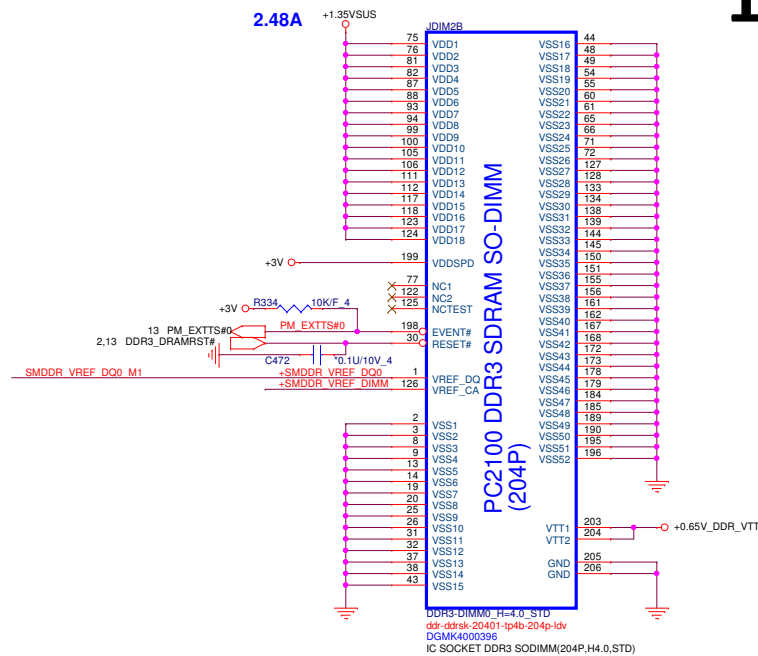




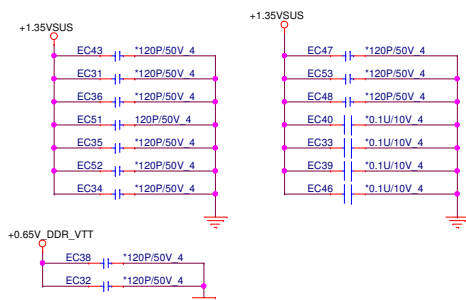
DIMM & Footprint 同Joshua提供



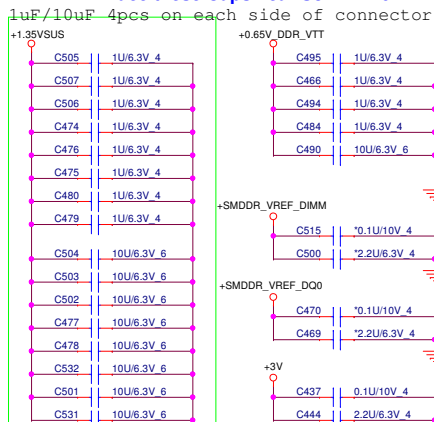
M_A_DQ[63:0] 3



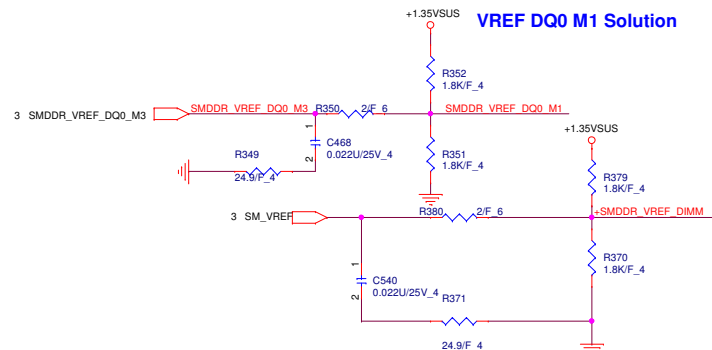
For EMI RESERVE



Place these Caps near So-Dimm0.

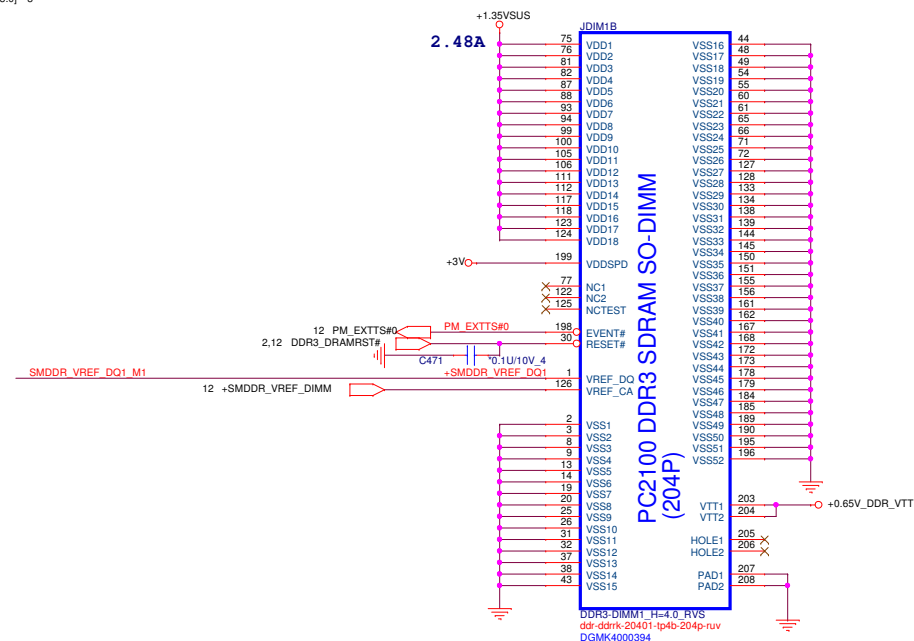
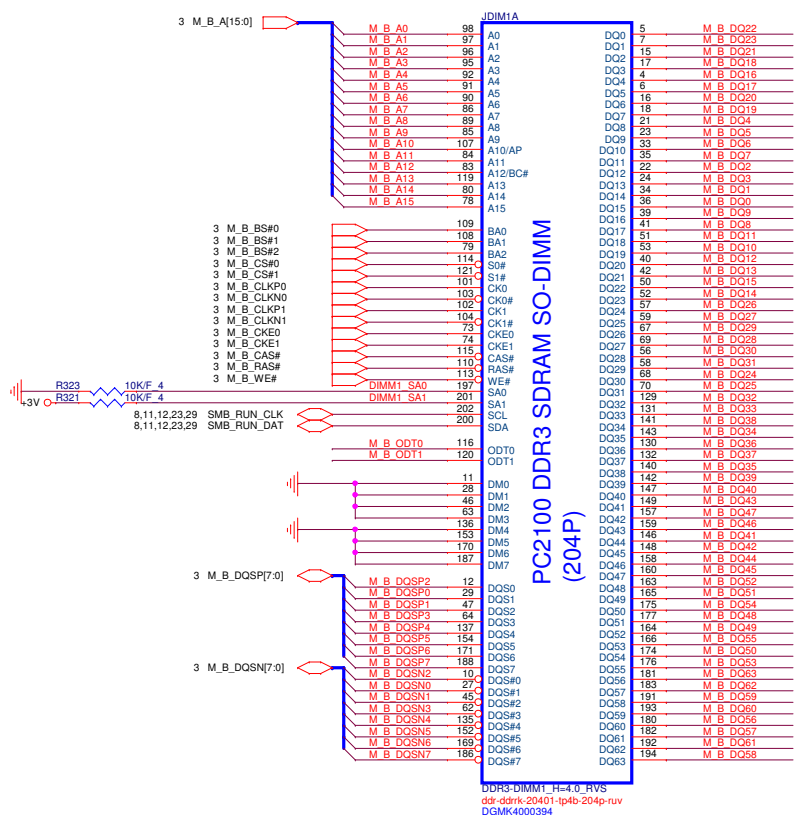


VREF DQ0 M1 Solution



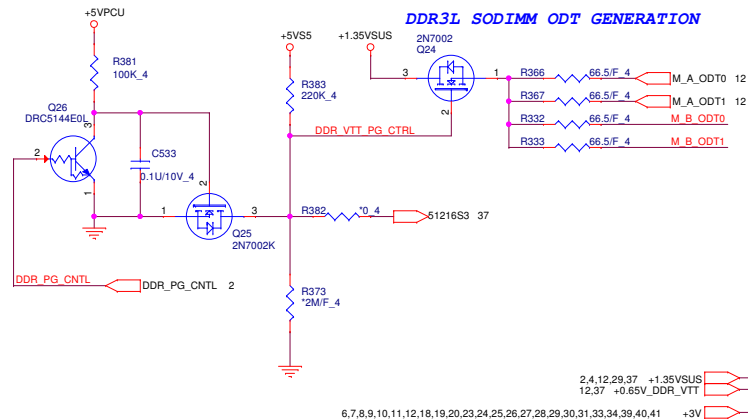
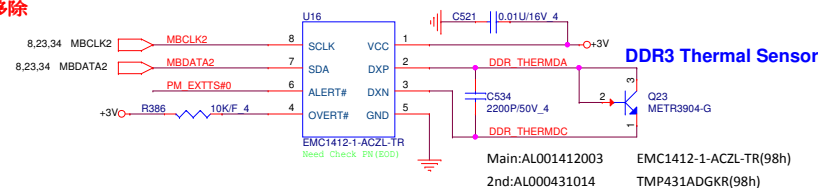
PROJECT : Y11C
Quanta Computer Inc.

Size Custom Document Number
DDR3 DIMM0-STD(4.0H)
Date: Friday, February 14, 2014 Sheet 12 of 44



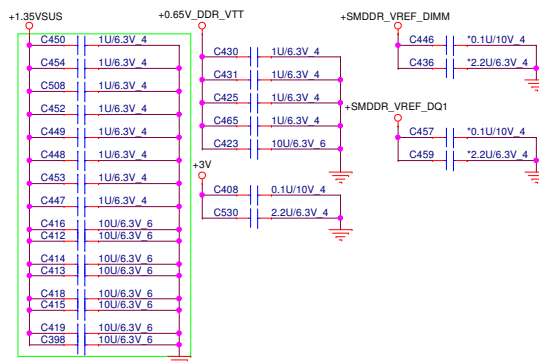
Local Thermal Sensor

MV可移除

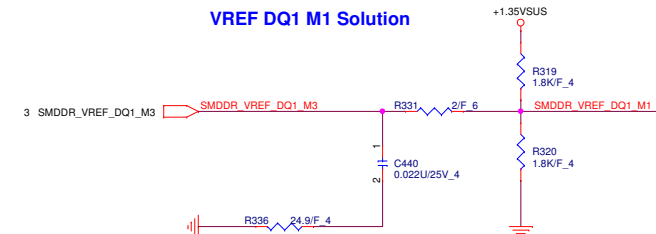


Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector

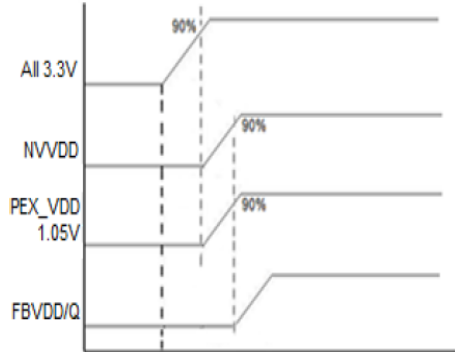
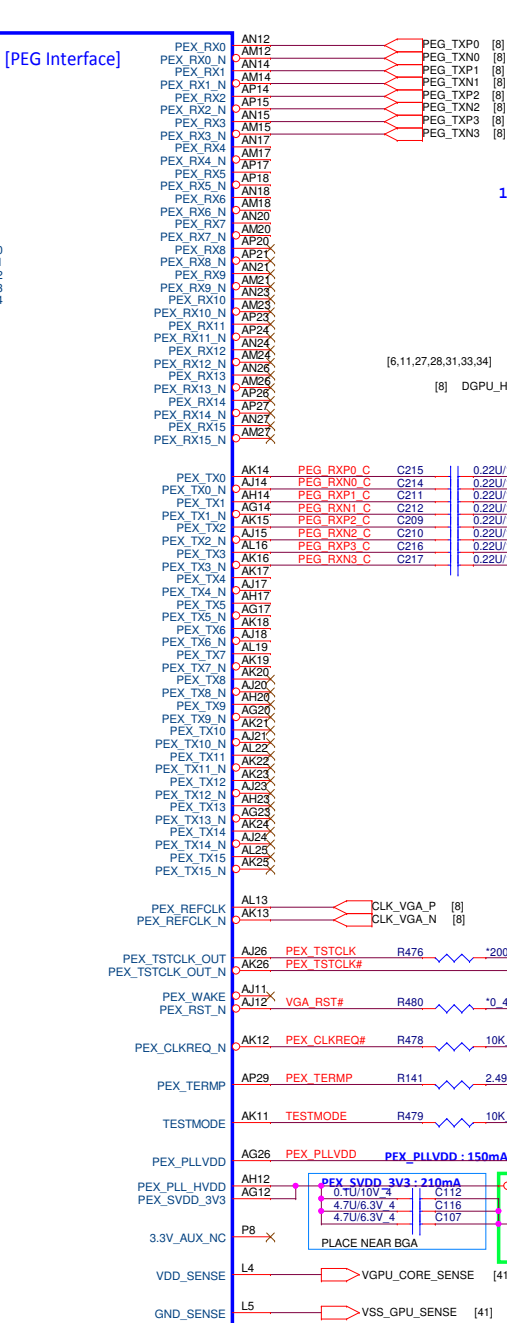


VREF DQ1 M1 Solution




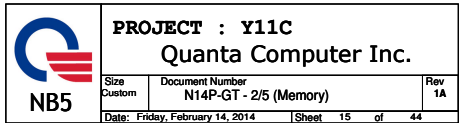
PROJECT : Y11C
Quanta Computer Inc.

Size Custom	Document Number DDR3 DIMM1-RVS(4.0H)	Rev 1A
Date: Friday, February 14, 2014	Sheet 13 of	44

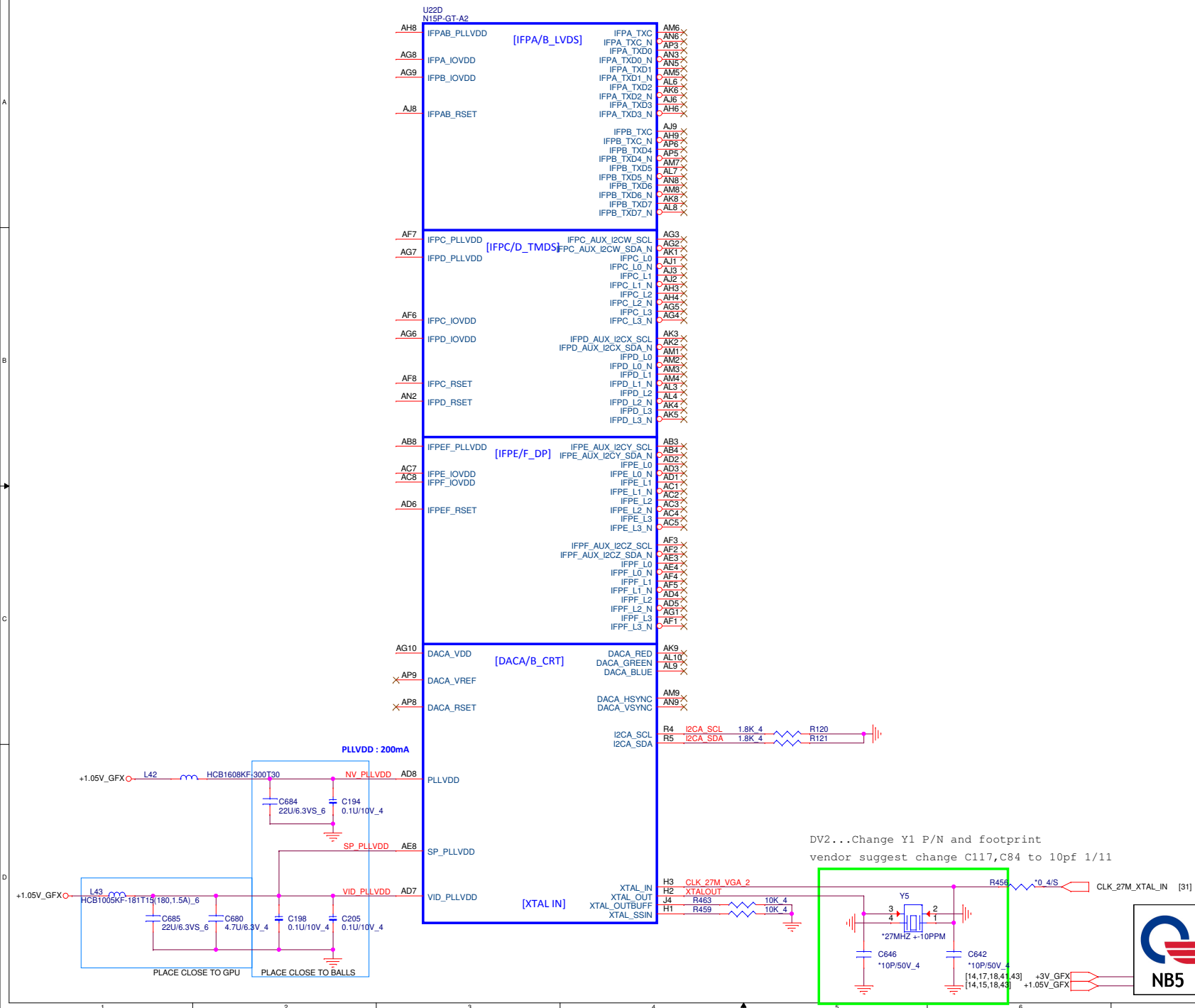


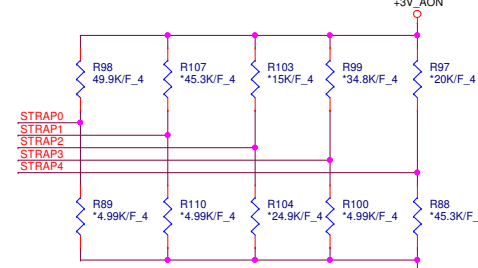
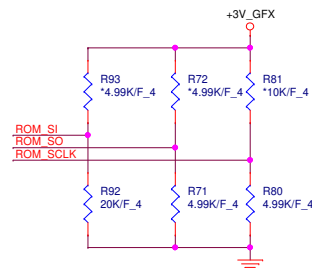
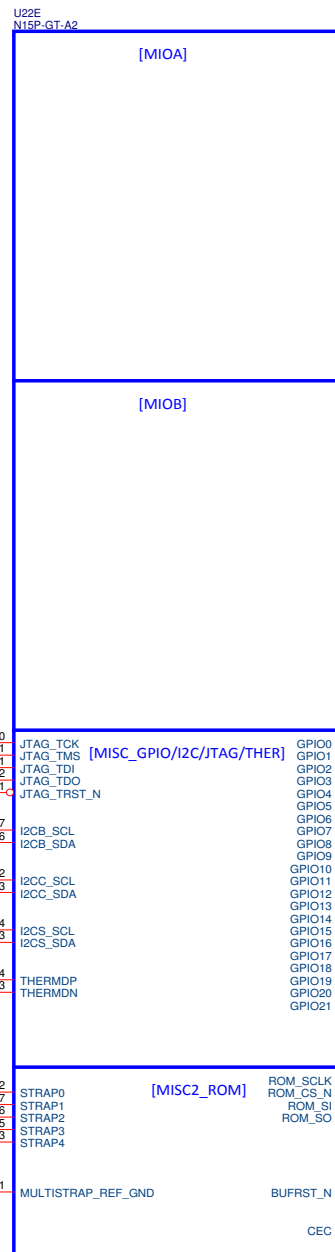
Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

 NB5	PROJECT : Y11C Quanta Computer Inc.		
	Size A3	Document Number N14P-GT - 1/5 (PCIE)	Rev 1A
	Date: Friday, February 14, 2014 Sheet 14 of 44		



Size A3	Document Number N14P-GT - 3/5 (Display)	Rev 1A
Date: Friday, February 14, 2014	Sheet 16 of 44	





Default: Hynix 2G VRAM

Vendor	Q : P/N	Mfr. P/N	ROM_SI	H.P
Hynix (1.35V)		H5TC4G63AFR-11C	0011	20K PD
Micron (1.35V)		MT41J256M16HA-093G:E	0100	24.9K PD
Samsung (1.35V)		K4W4G1646D-BC1A	0101	30.1K PD

N15P-GT device ID=0x1391

Netname	N15P-GT
ROM_SO	4.99K PD
ROM_SCLK	4.99K PD
STRAP0	49.9K PU
STRAP1	NC
STRAP2	NC
STRAP3	NC
STRAP4	NC

4.99K/F 4: CS24992FB26 RES CHIP 4.99K 1/16W +1%(0402)
 10K/F 4: CS31002FB26 RES CHIP 10K 1/16W +1%(0402)
 15K/F 4: CS31002FB24 RES CHIP 15K 1/16W +1%(0402)
 20K/F 4: CS32002FB29 RES CHIP 20K 1/16W +1%(0402)
 24.9K/F 4: CS32492FB16 RES CHIP 24.9K 1/16W +1%(0402)
 30.1K/F 4: CS33012FB18 RES CHIP 30.1K 1/16W +1%(0402)
 34.8K/F 4: CS33482FB22 RES CHIP 34.8K 1/16W +1%(0402)
 45.3K/F 4: CS34532FB18 RES CHIP 45.3K 1/16W +1%(0402)

Logical Strap Bit Mapping

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Table 15-4 GB3-256 Multi-Level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	PCI_DEVID[4]	SUB_VEHIDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

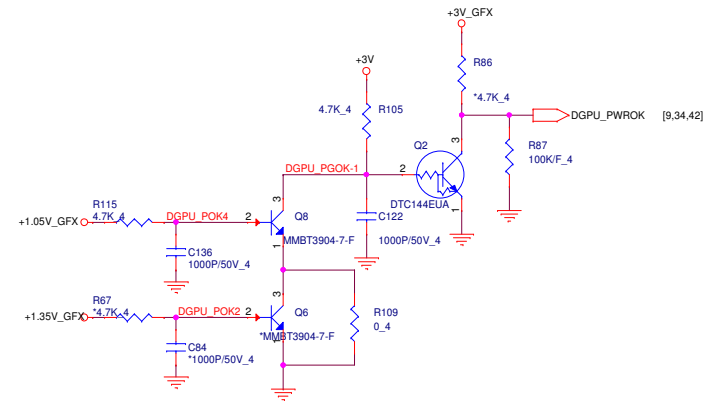
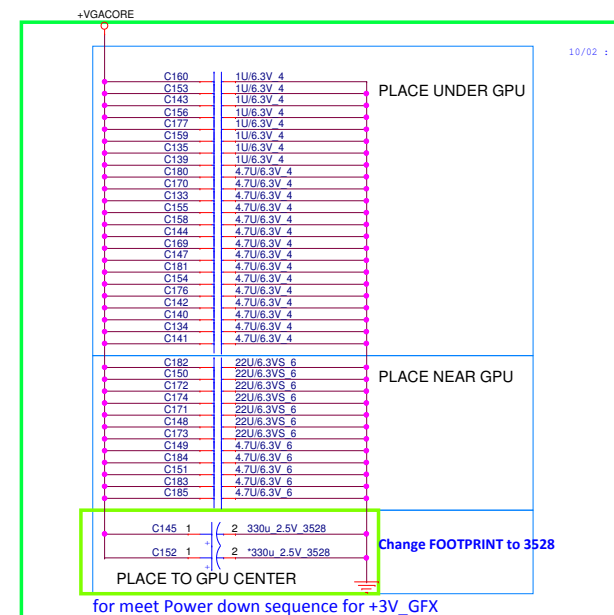
Table 28. H155-GX and H15P-GT DDR3L Recommended Memories 256Mx16 Configuration

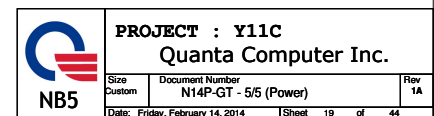
Configuration	Vendor	Strap	FBVDD/FBVDDQ	Manufacturer Part Number	Max Speed CLK (MHz)	Memory Date Code Minimum	Status
256M:16 DDR3L	Hynix	0x3	1.35 V/1.35 V	H5TC4G63AFR-11C	900	I/A	Production candidate
	Micron	0x4	1.35 V/1.35 V	MT41J256M16HA-093G:E	900	1322	Production candidate
	Samsung	0x5	1.35V/1.35V	K4W4G1646D-BC1A	900	I/A	Post-production candidate

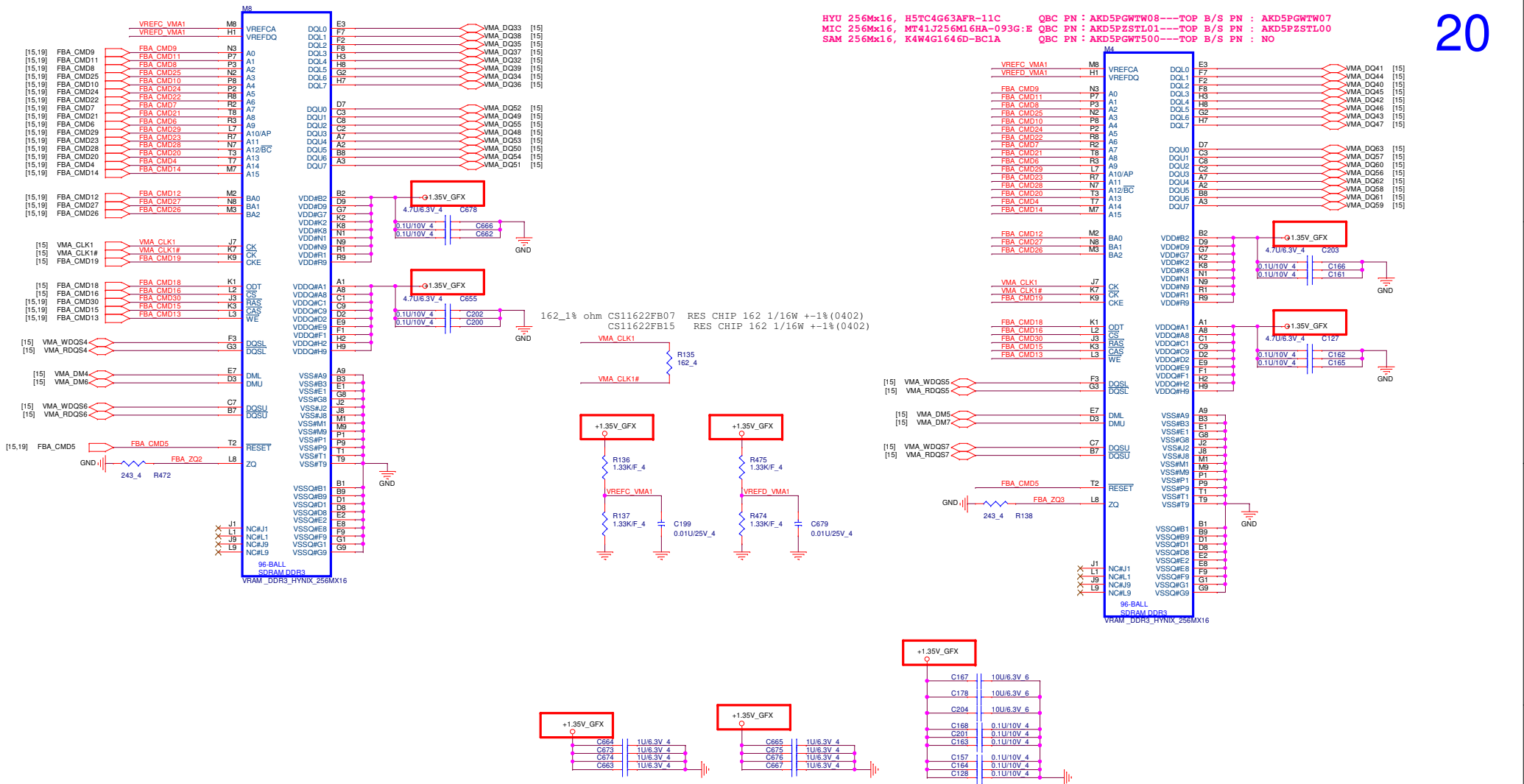
GPIO ASSIGNMENTS

GPIO	GPIO7/GM08	GPIO10/GK107
GPIO 0	GC6_FB_EN	GPIO_FB_CLAMP
GPIO 1	MEM_VDD_CTL	MEM_VDD_CTL
GPIO 2	LCD_BL_PWM	LCD_BL_PWM
GPIO 3	LCD_PWM_EN	LCD_PWM_EN
GPIO 4	LCD_BLEN	LCD_BLEN
GPIO 5	GC6_PWM_EN	DEBUG SERVICE HEADER
GPIO 6	GPU_EVENT*	Remote Sensor Error Correction
GPIO 7	DEBUG SERVICE HEADER	3D STEREO
GPIO 8	SYS_PEX_RST_MON*	GPU OVERTEMP
GPIO 9	Remote Sensor Error Correction	GPU THERMAL ALERT/FAN_PWM
GPIO 10	MEM_VREF_CTL(N/A)	MEM_VREF_CTL
GPIO 11	WVDD_PMM_VID	WVDD_PMM_VID
GPIO 12	AC DETECT	AC DETECT
GPIO 13	WVDD_PSI	WVDD_PSI
GPIO 14	IFPD_HDP	N/C
GPIO 15	N/C	N/C
GPIO 16	FRAME LOCK	FRAME LOCK
GPIO 17	IFPD_HDP(DP)	IFPD_HDP(DP1M)
GPIO 18	IFPD_HDP(DP1M)	IFPD_HDP(DP1M)
GPIO 19	IFPD_HDP(DP1M)	IFPD_HDP(DP1M)
GPIO 20	GC6_MODE	N/A
GPIO 21	GPU_PEX_RST_HOLD*	N/A

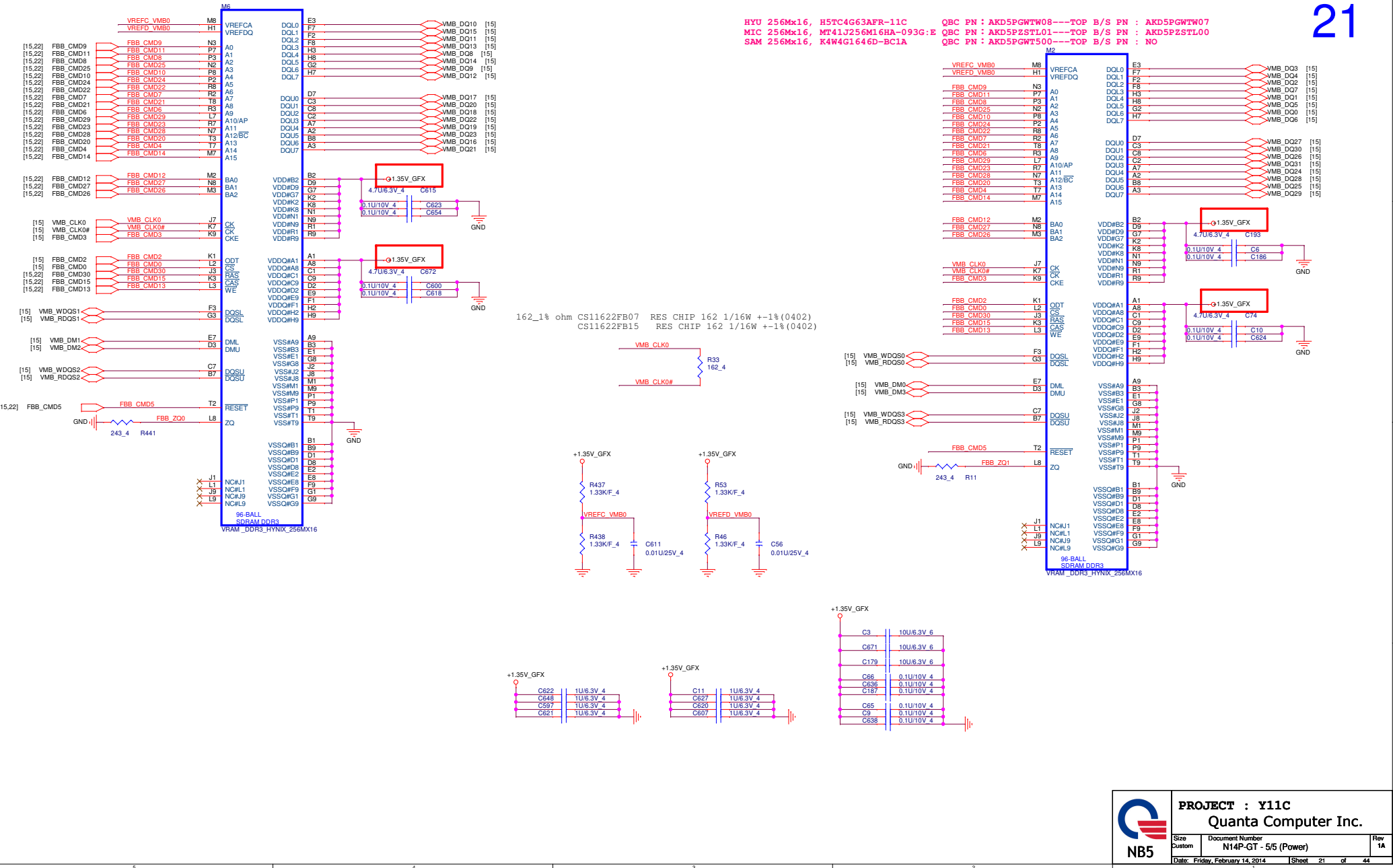
		PROJECT : Y11C		Rev 1A
		Quanta Computer Inc.		
Size Custom	Document Number N14P-GT - 4/5 (MISC)	Date: Friday, February 14, 2014	Sheet 17 of 44	

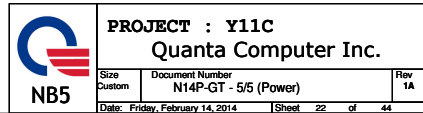




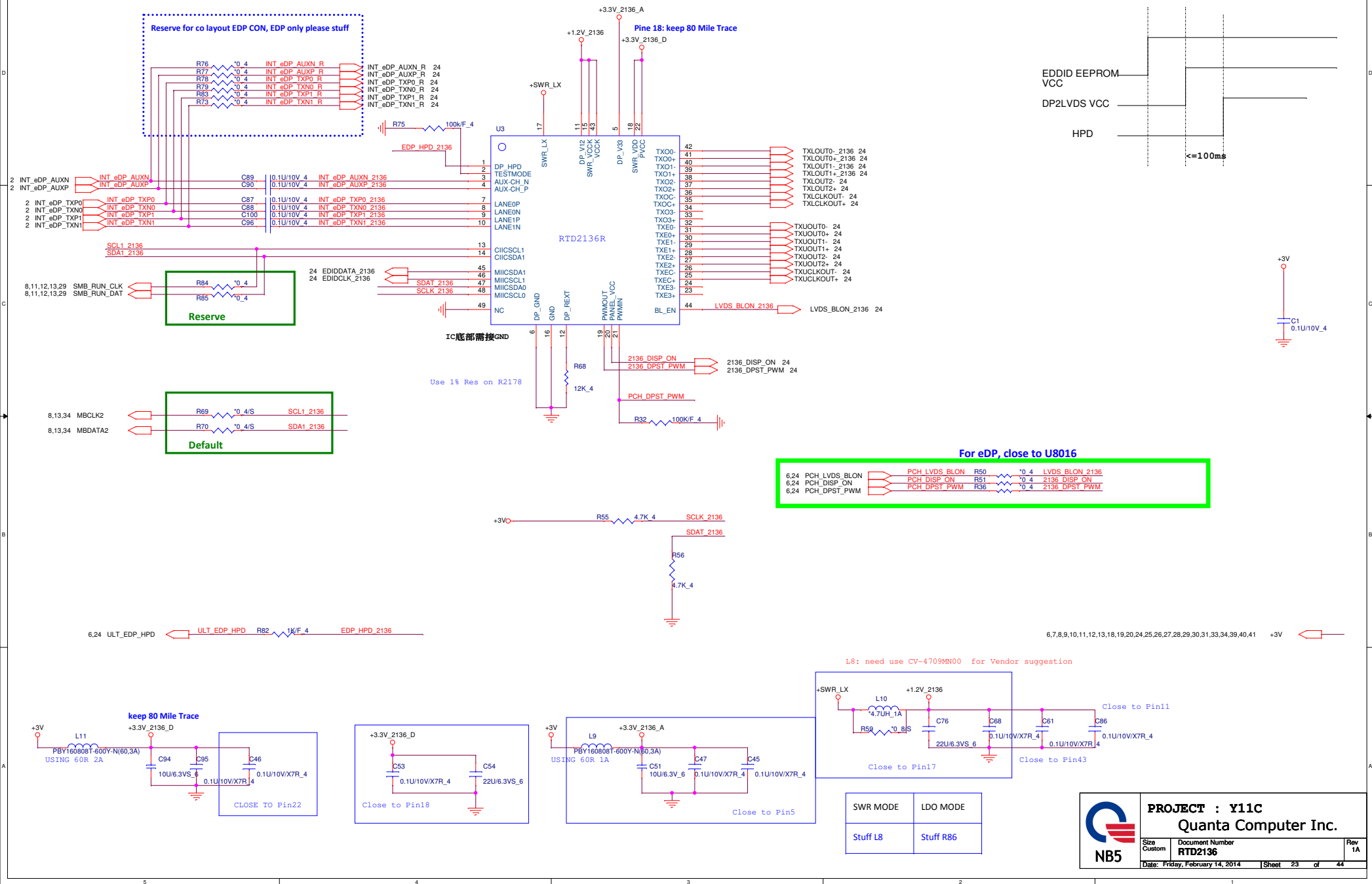


HYU 256Mx16, H5TC4G63AFR-11C QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT500---TOP B/S PN : NO

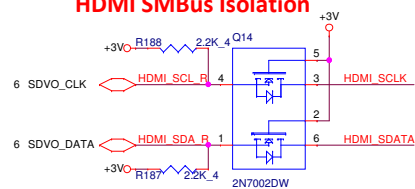
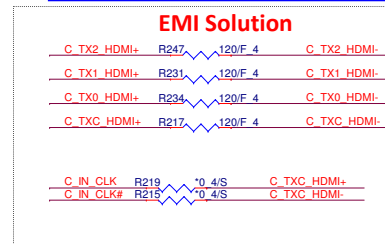
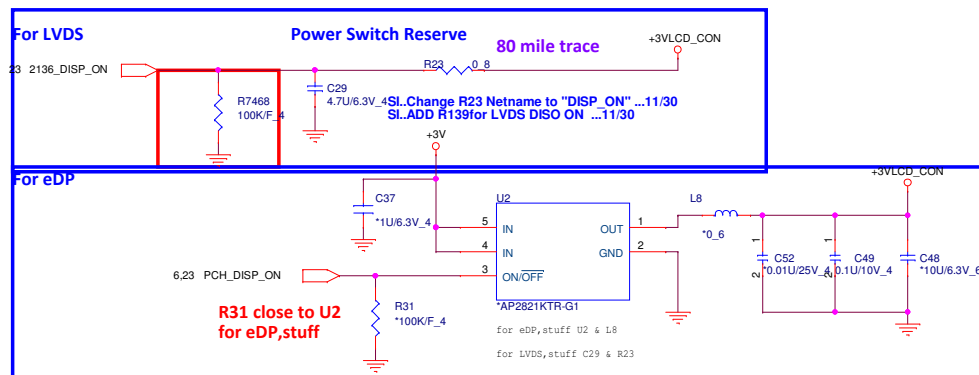
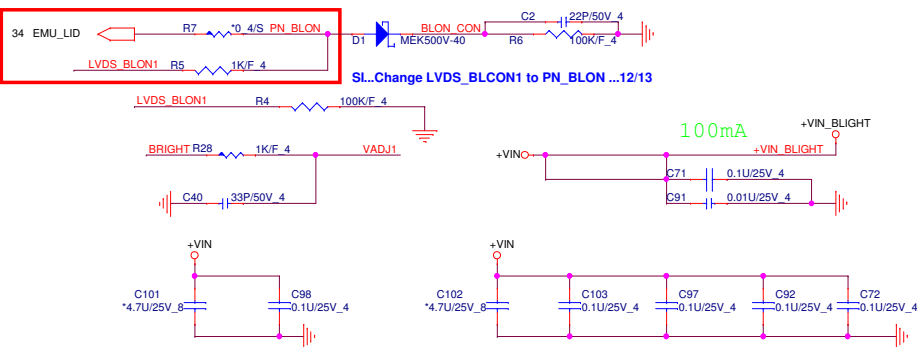




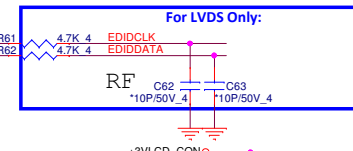
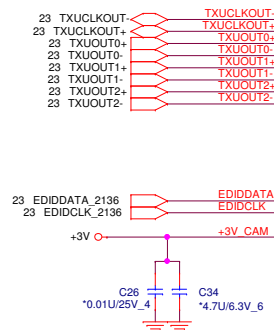
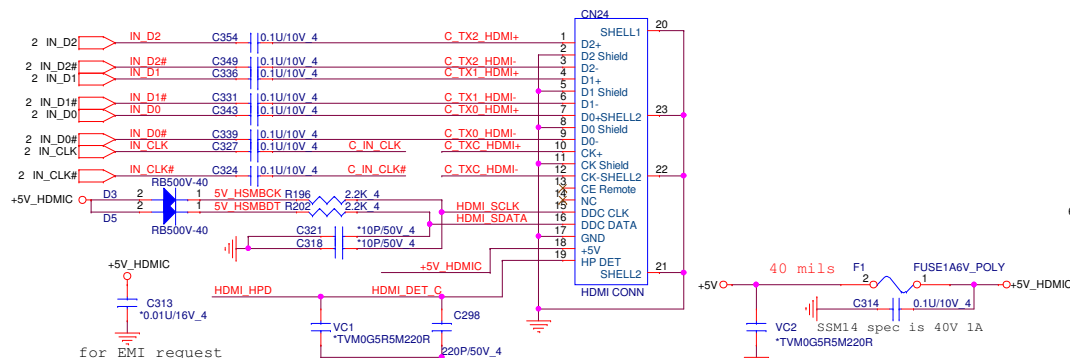
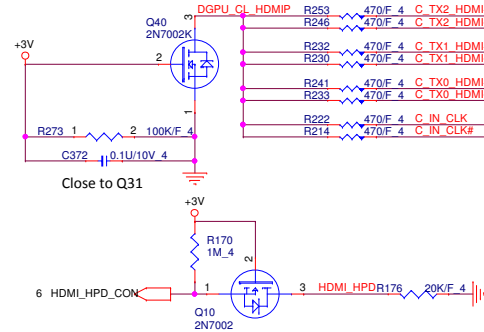
RTD2136 Dual Channel only



LID Switch

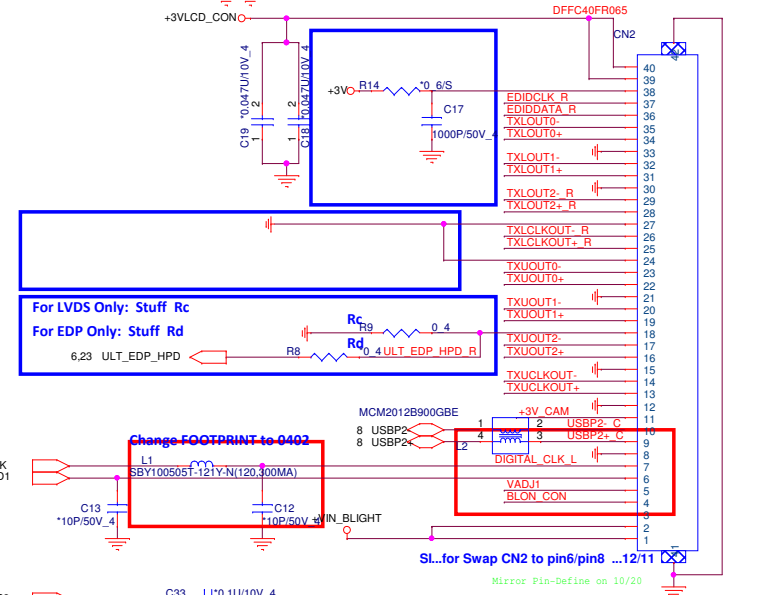


For EDP Only: stuff Cap
For LVDS only stuff Resistor

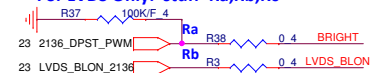
**LVDS Conn.**

24

GS12401-1011-9H
lvs-50671-04041-001-40p-l



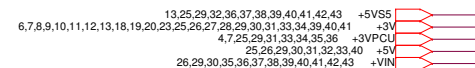
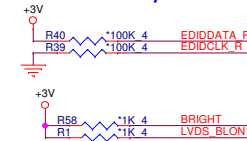
For LVDS Only: stuff Ra,Rb,Rc



For EDP Only: stuff Rd,Re,Rf



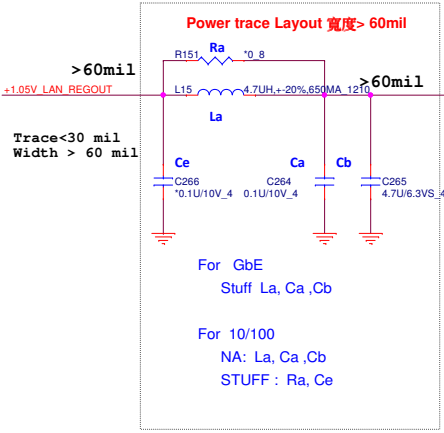
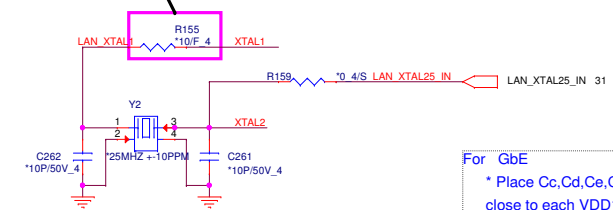
For EDP Only: stuff



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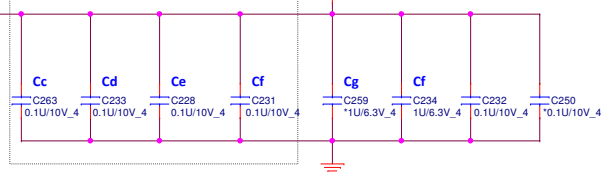
Size Custom	Document Number LCD CONN/LID/CAM/D-MIC	Rev 1.
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For EMI 0 ~ 22 ohm



For GbE
* Place Cc, Cd, Ce, Cf, C232
close to each VDD10 pin-- 3, 22, 8, 30

For 10/100 NA Ce, Cf
* Place Ce, Cf, C250
close to each VDD10 pin-- 8, 30 only,

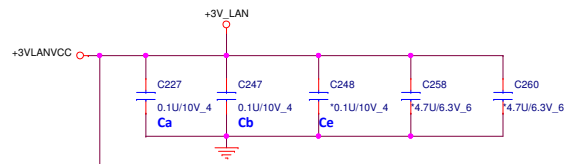


For GbE
* Place Cf close to each VDD10 pin-- 22 (reserve)

For 10/100
* Place Cg close to each VDD10 pin-- 30 (reserve)

For 10/100
* Stuff Cb and Ce only, close to each VDD33 pin-- 23, 32

For GIGA
* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32

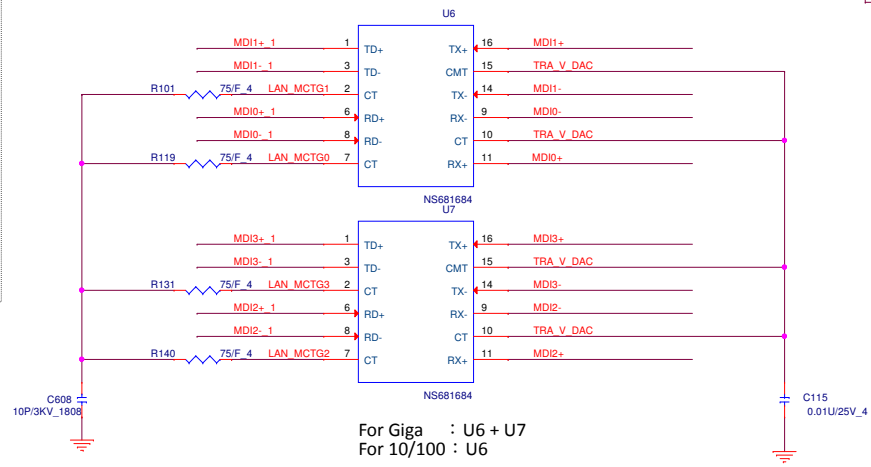


* Place Cc and Cd close to each VDD33 pin-- 23

For GIGA
Stuff Cc, Cd

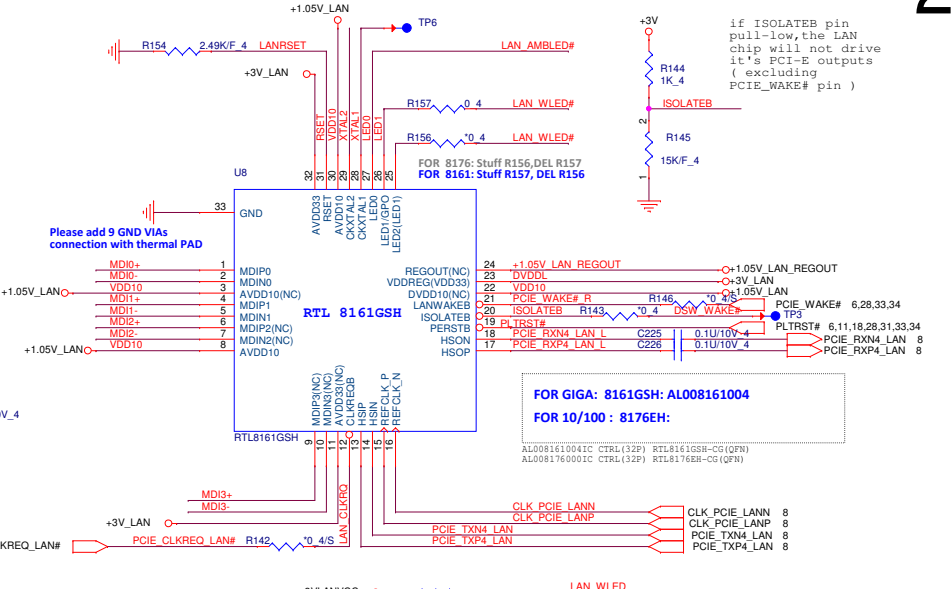
For 10/100
NA: Cc, Cd

Remove For Not Using SWR mode



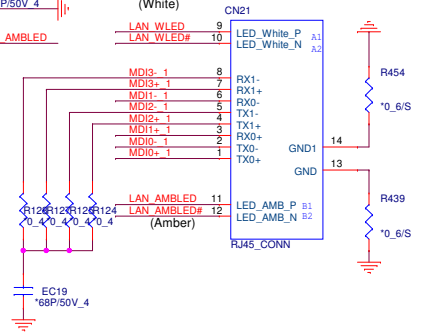
6,7,8,9,10,11,12,13,18,19,20,23,24,25,26,28,29,30,31,33,34,39,40,41

+3V
31,40 +3VLANVCC

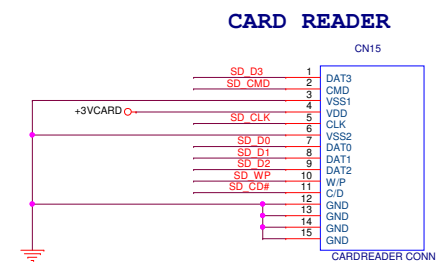
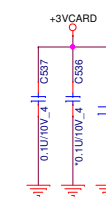
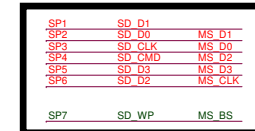
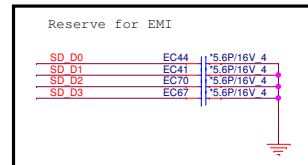
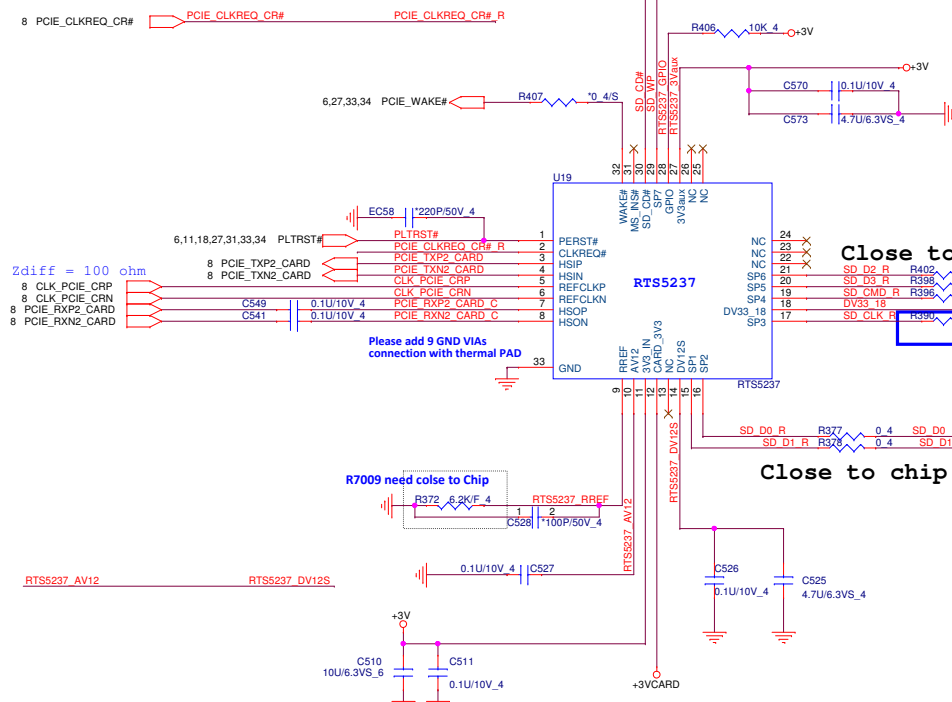


if ISOLATEB pin
pull-low, the LAN
chip will not drive
it's PCI-E outputs
(excluding
PCI-E_WAKE# pin)

RJ45

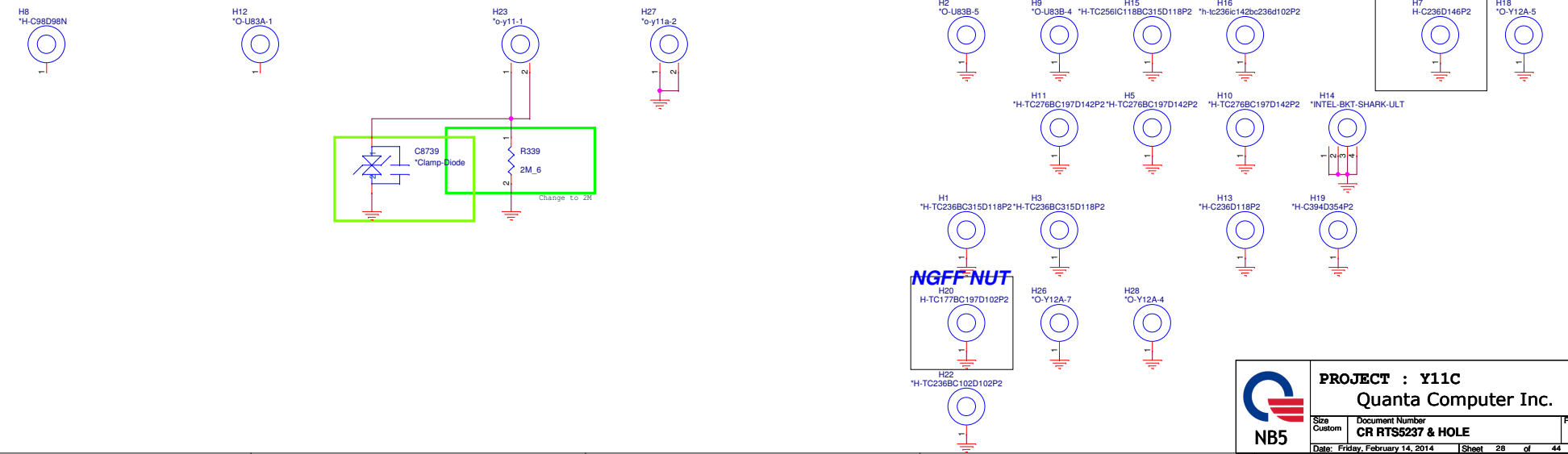


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	Quanta Computer Inc.		
	Size Custom	Document Number	Rev 1A
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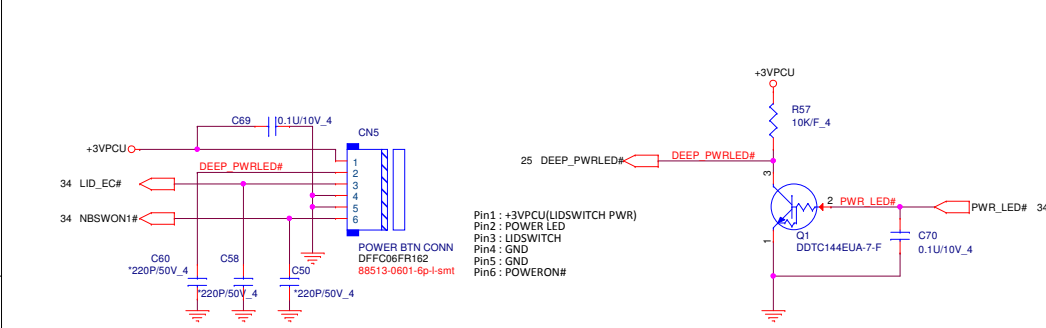


R6x Type

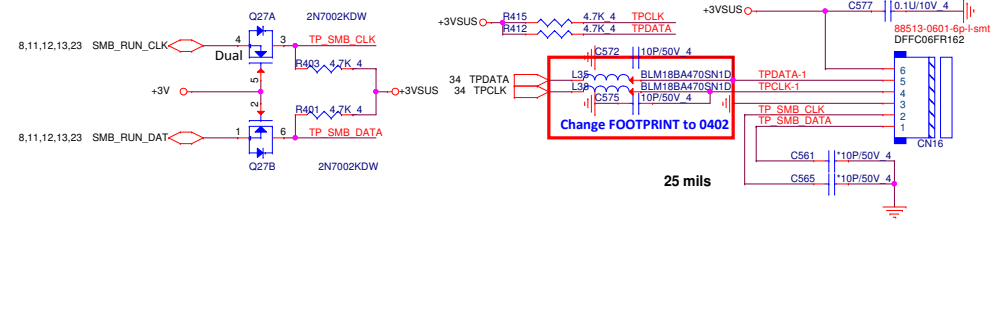
Thermal Nut



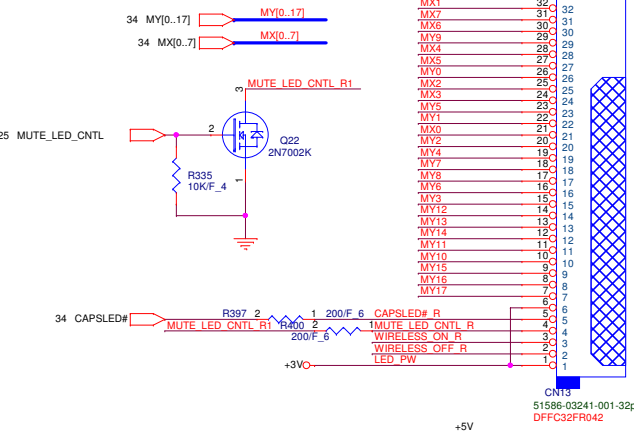
Power Button Connector



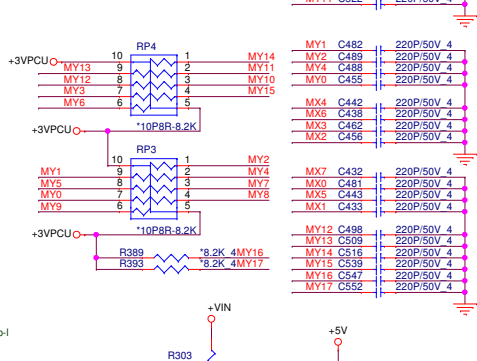
Touch Pad Connector



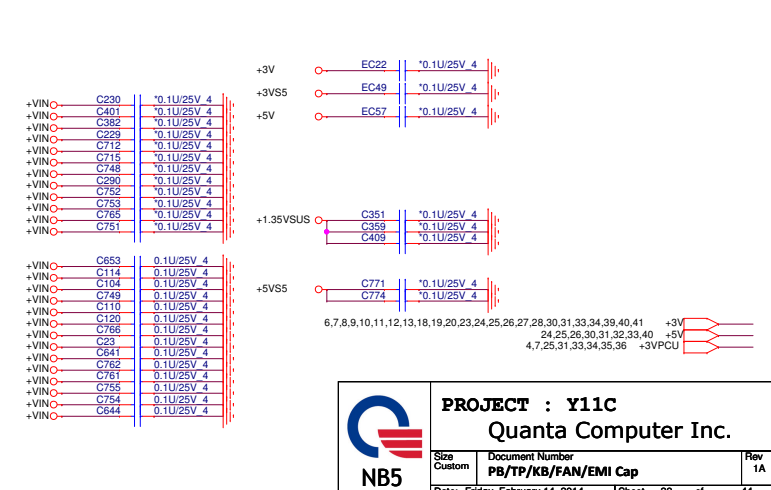
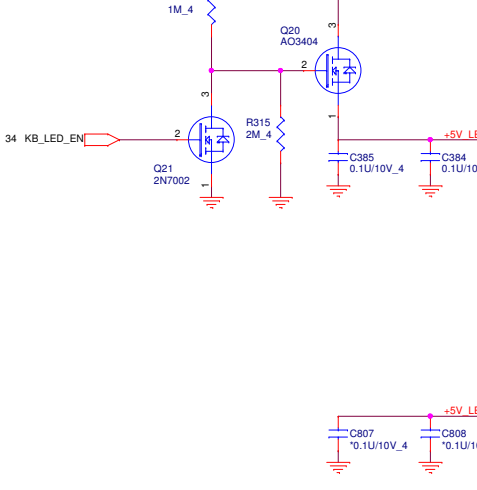
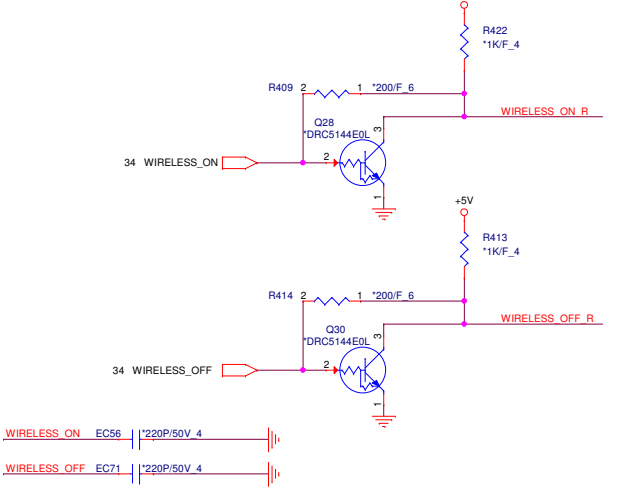
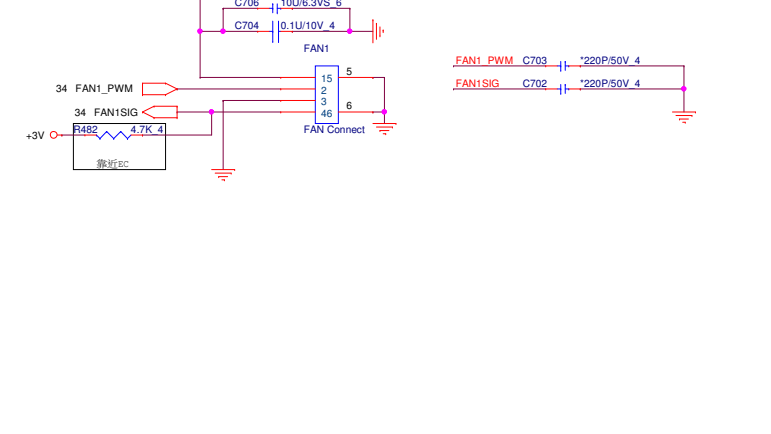
KEYBOARD Con.



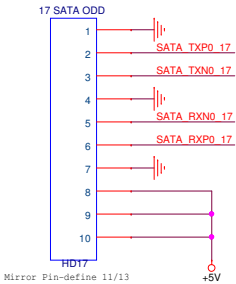
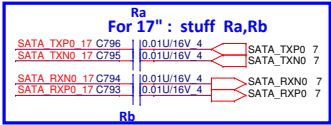
KEYBOARD PULL-UP



FAN

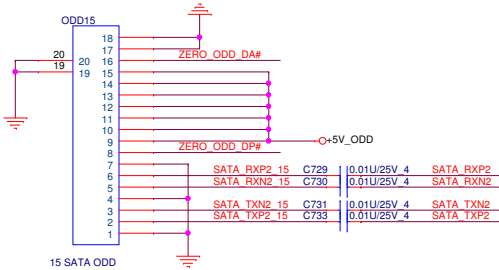


SATA HDD Connector(Cable type) 15.6"



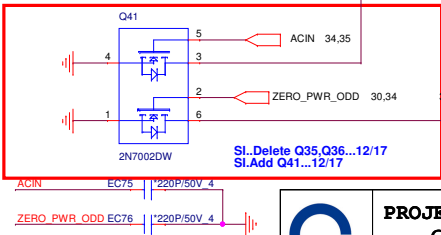
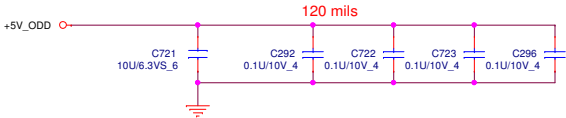
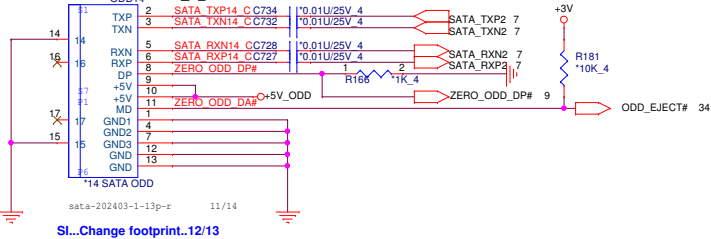
SATA ODD
CONNECTOR

15" SATA ODD



14" SATA ODD

Bypass CAP close conn



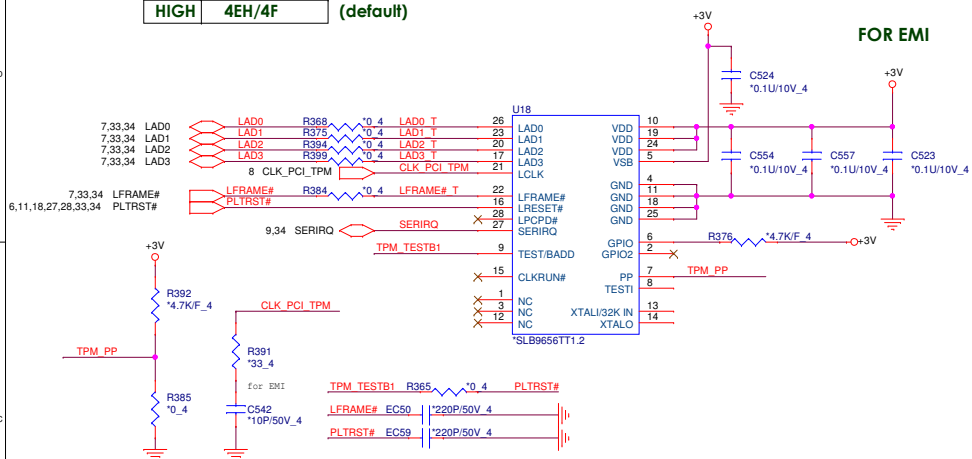
High : ODD power down
Low : ODD power on

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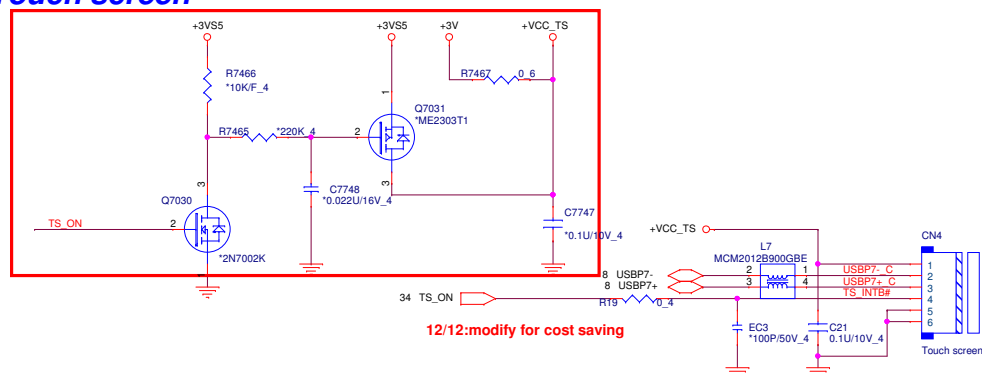
Size Custom	Document Number HDMI	Rev 1A
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Address

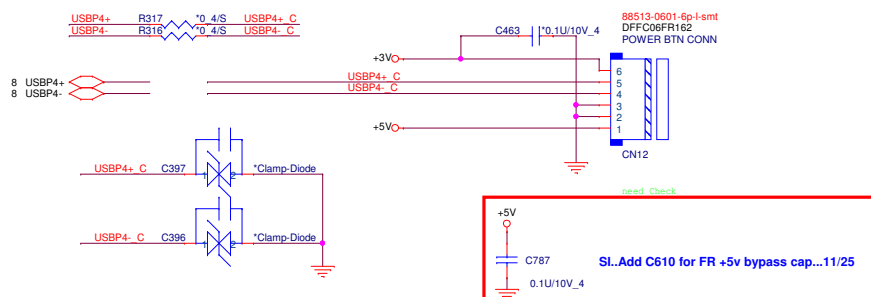
	BADD
HIGH	4EH/4F (default)



Touch screen

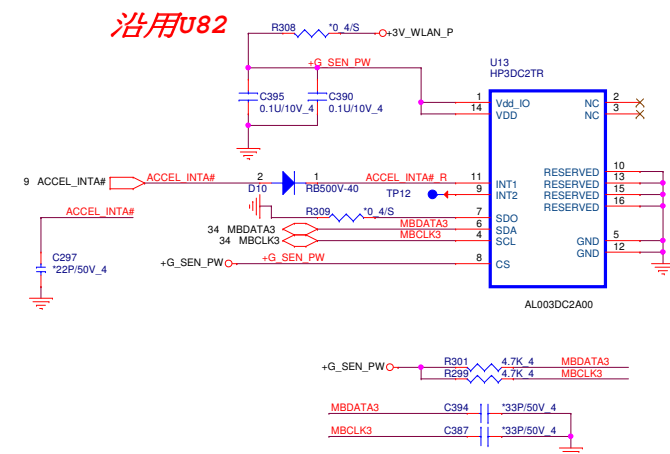


Fingerprint Conn

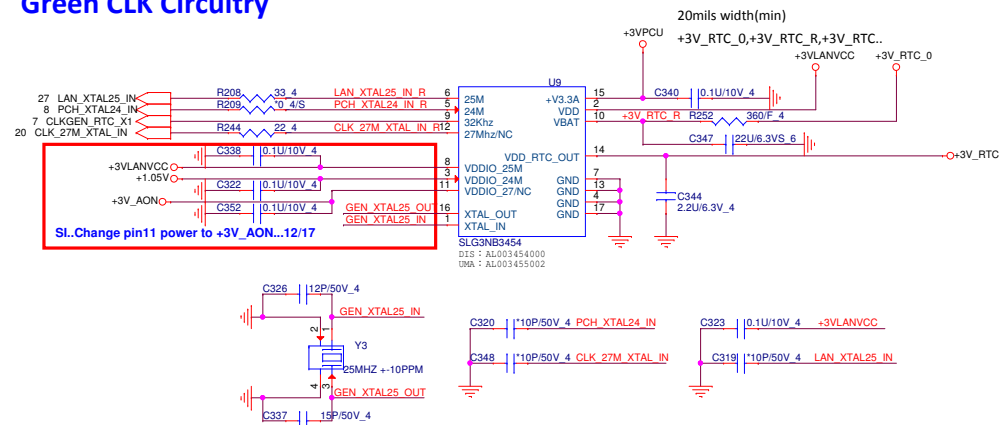


Accelerometer Sensor

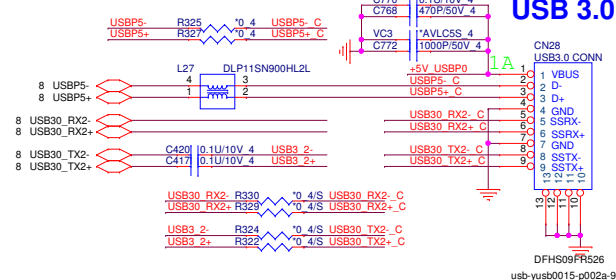
31



Green CLK Circuitry

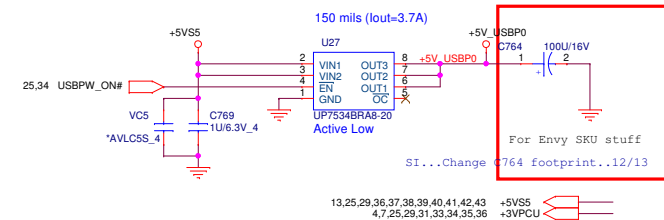
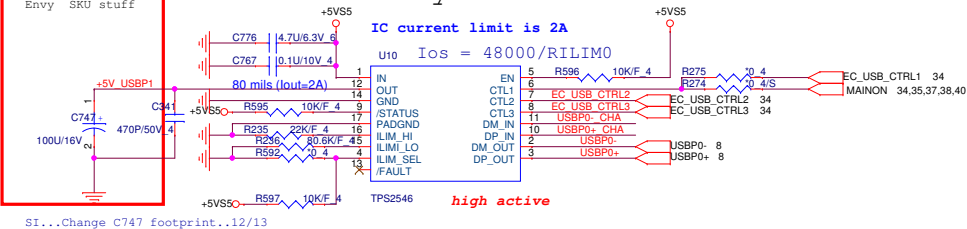


USB 3.0



for Envy SKU stuff

IC current limit is 2A



AEQ 9.5db / ADE 3.5db
BEQ 13db / BDE 5db / REXT 5.36K

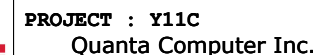
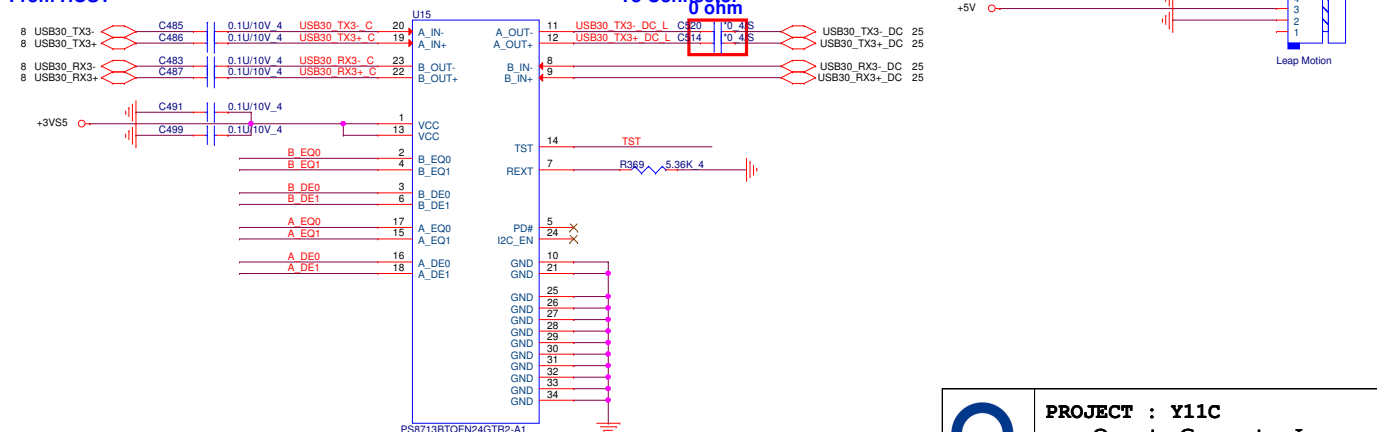
A_EQ1	A_EQ0		A_DE1	A_DE0	
B_EQ1	B_EQ0		B_DE1	B_DE0	
0	0	9.5dB	0	0	3.5dB
0	1	13dB	0	1	no de-emphasis
1	0	4.5dB	1	0	2.7dB
1	1	7.5dB	1	1	5dB

TST : Low = Normal LFPS swing / Hight =Turn down LFPS swing

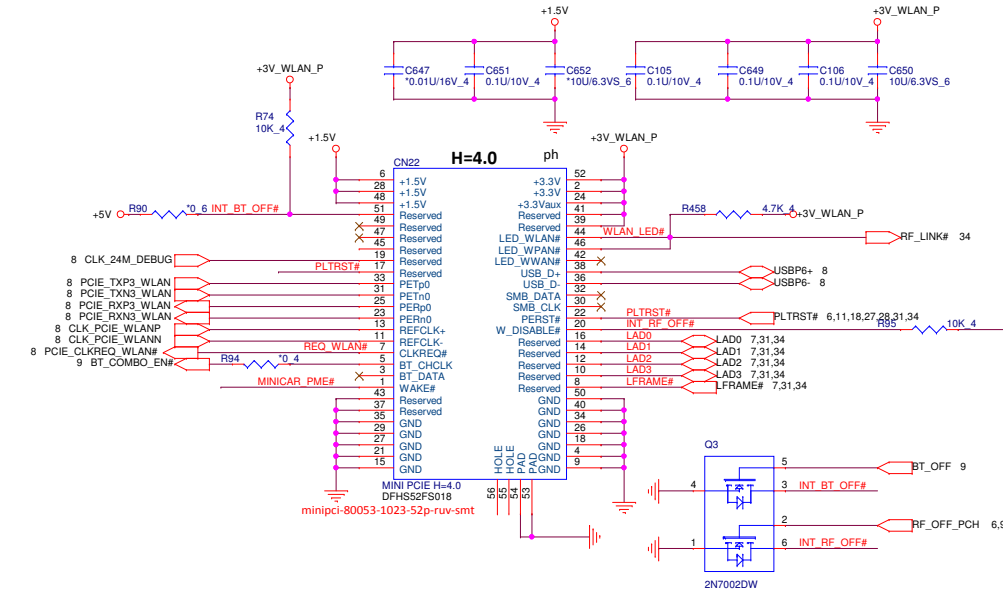
From HOST

USB3.0 Re-driver

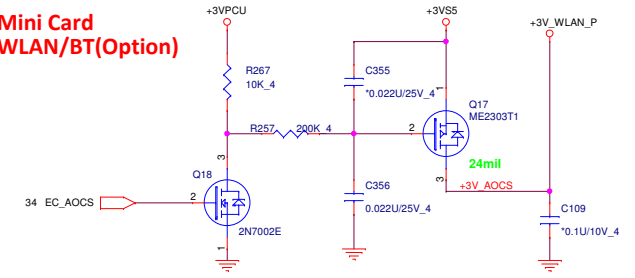
To Connector
0 ohm



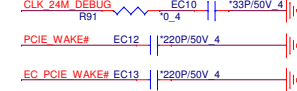
Size Custom	Document Number USB 3.0	Rev 1A
Date: Friday, February 14, 2014	Sheet 32 of	44



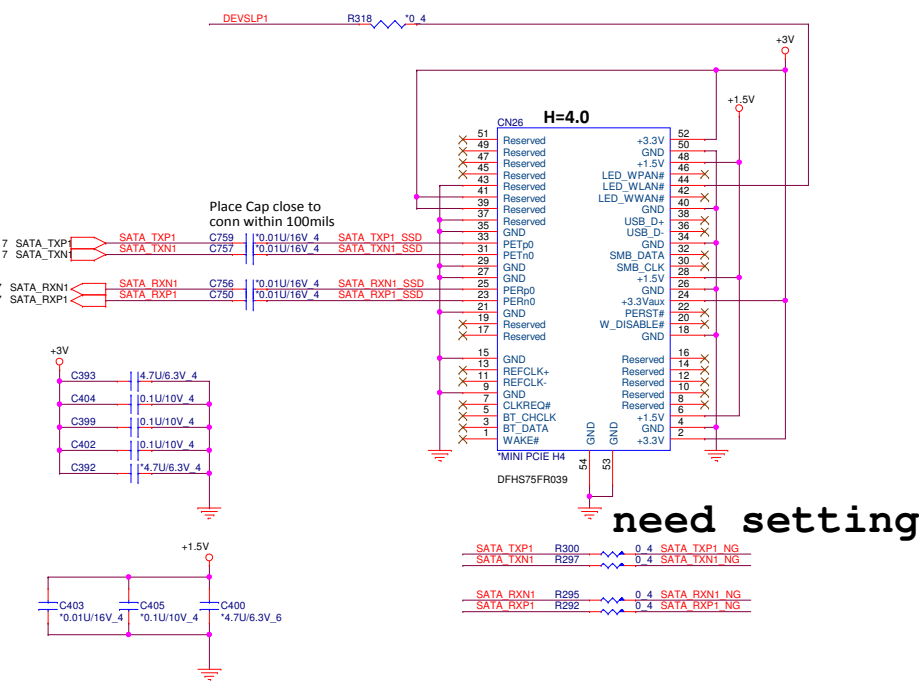
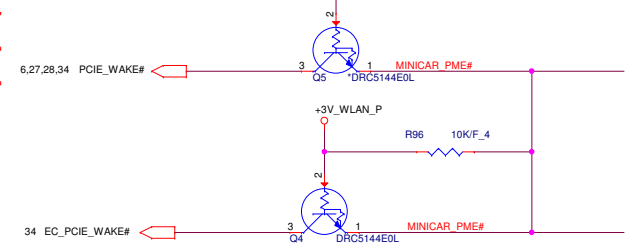
Mini Card
WLAN/BT(Optional)



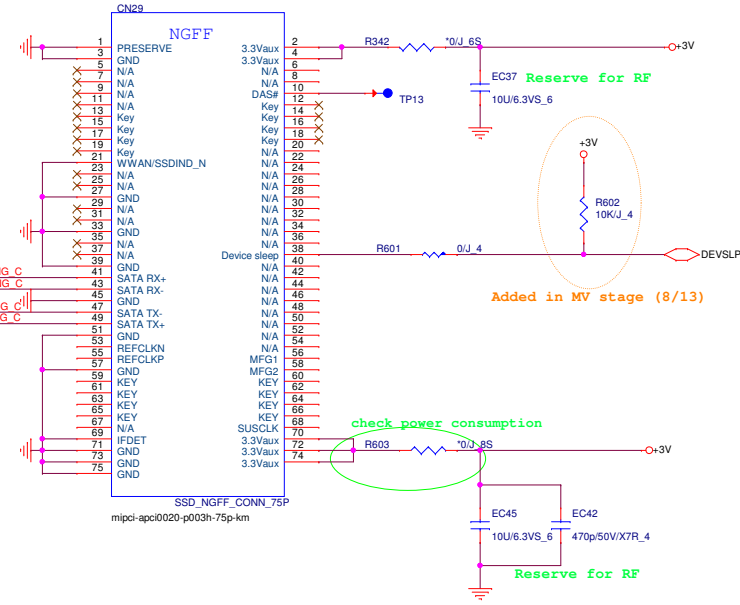
For EMI Suggestion



Support Wake Function(Reserve)



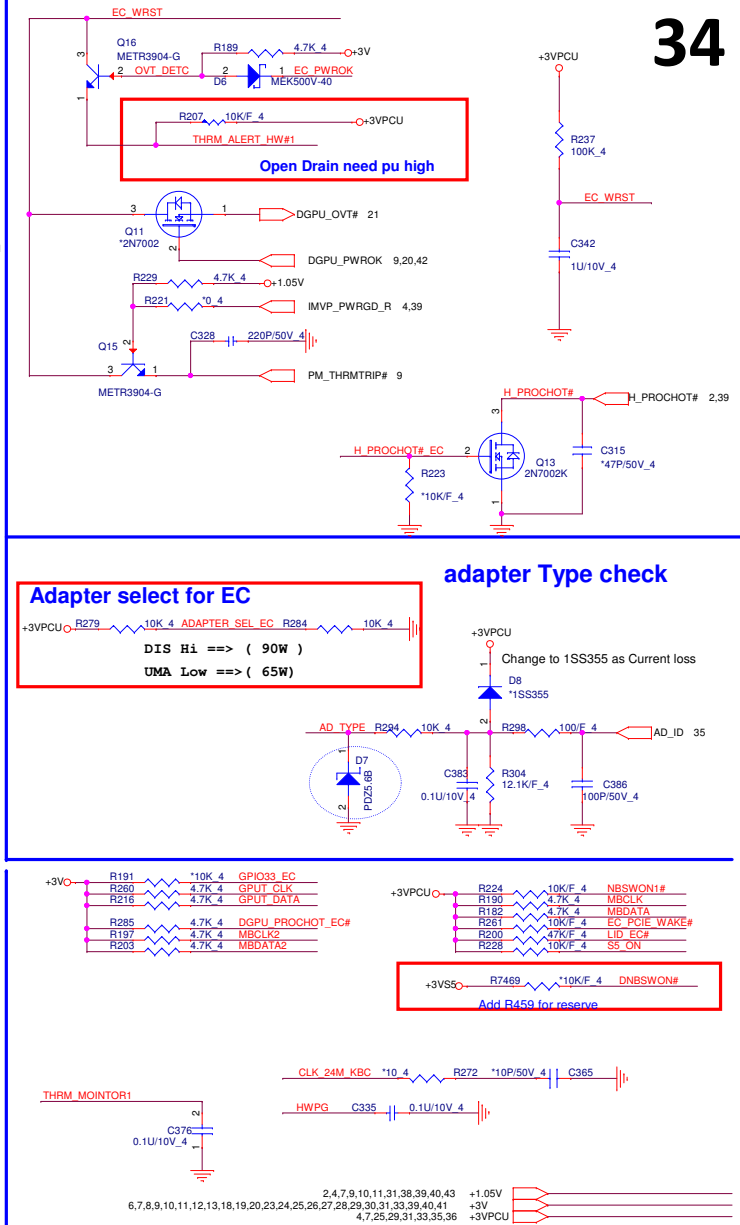
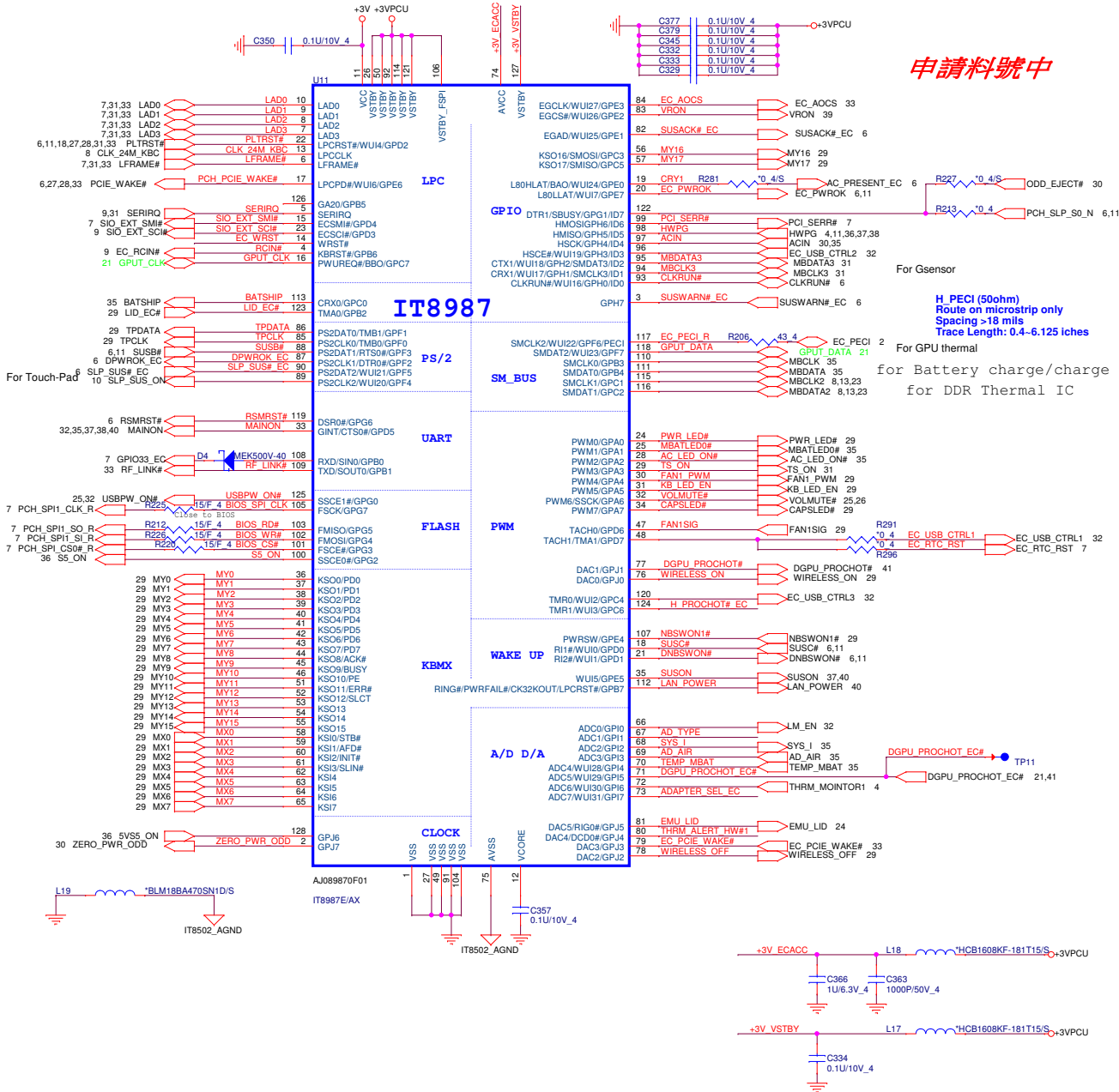
NGFF-SSD

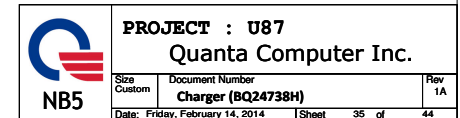


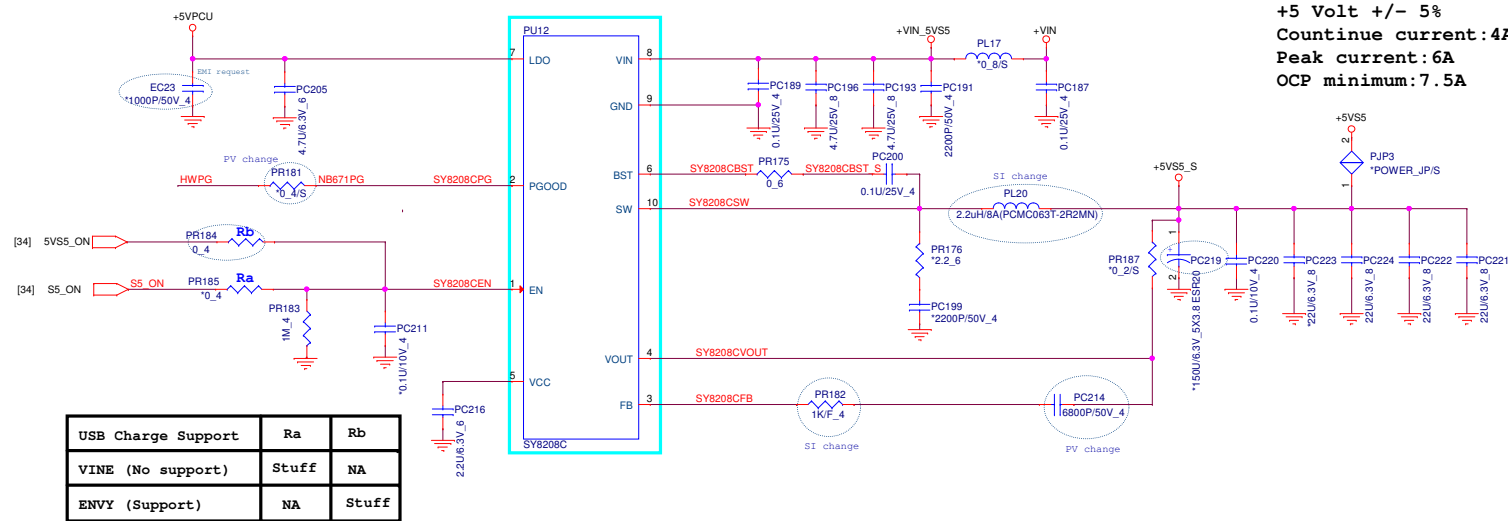
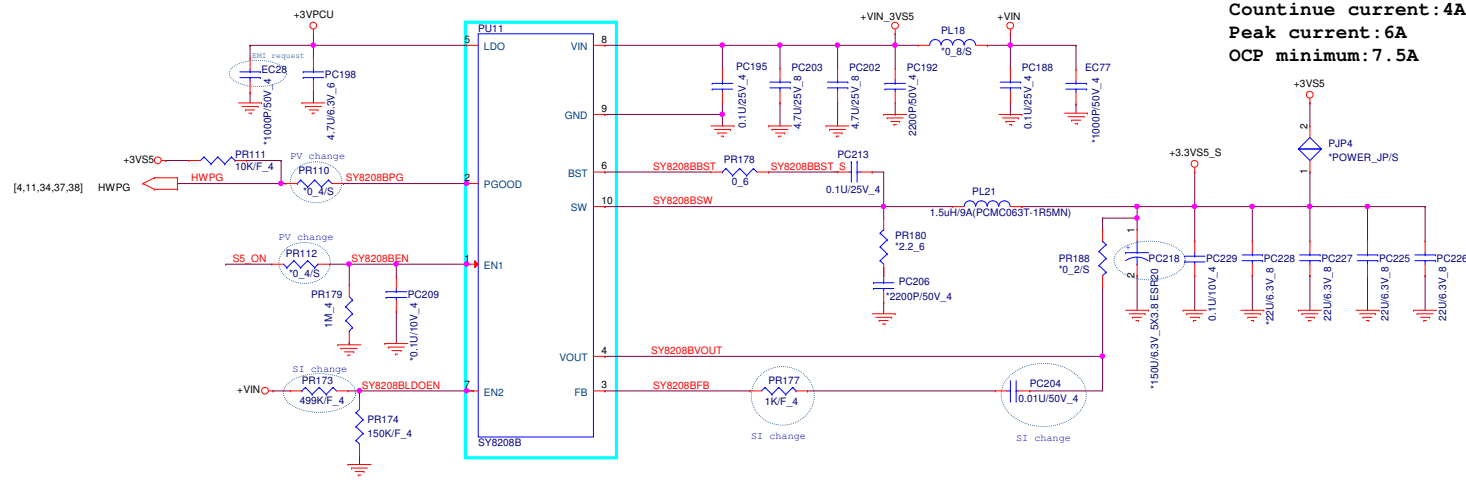
need setting

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Size	Custom	Document Number	WLAN/NGFF/MSATA
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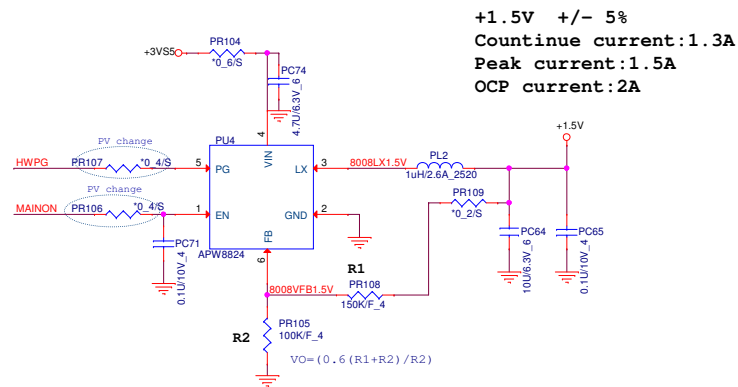
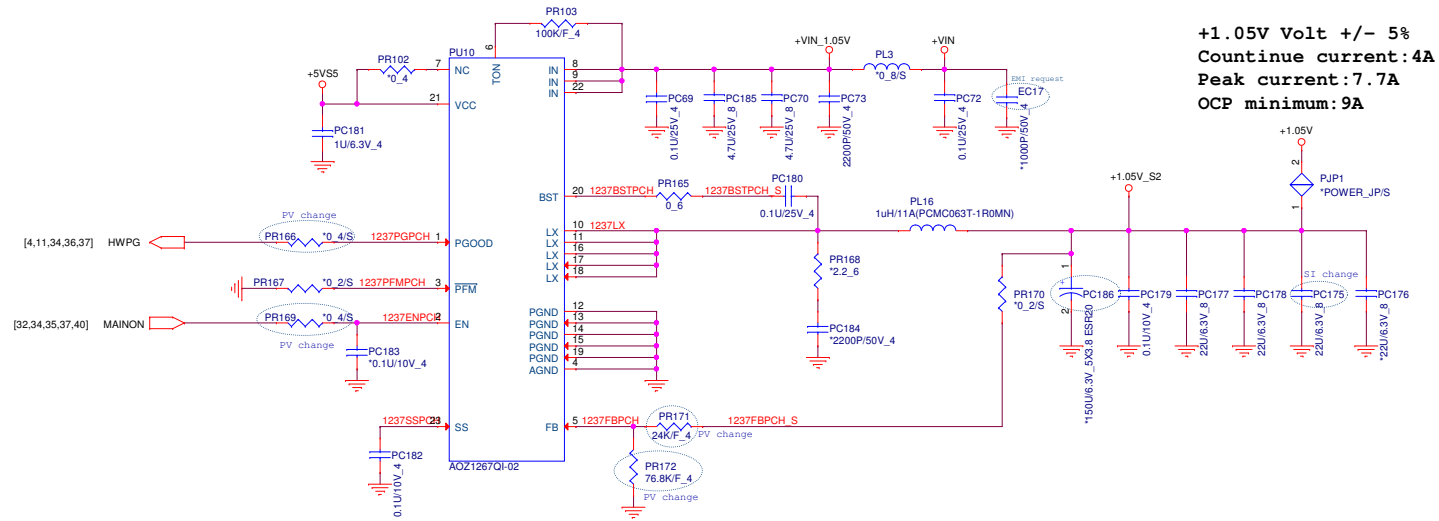
6,7,8,9,10,11,12,13,18,19,20,23,24,25,26,27,28,29,30,31,34,39,40,41
24,25,26,29,30,31,32,40 +5V
4,7,25,29,31,34,35,36 +3VPCU











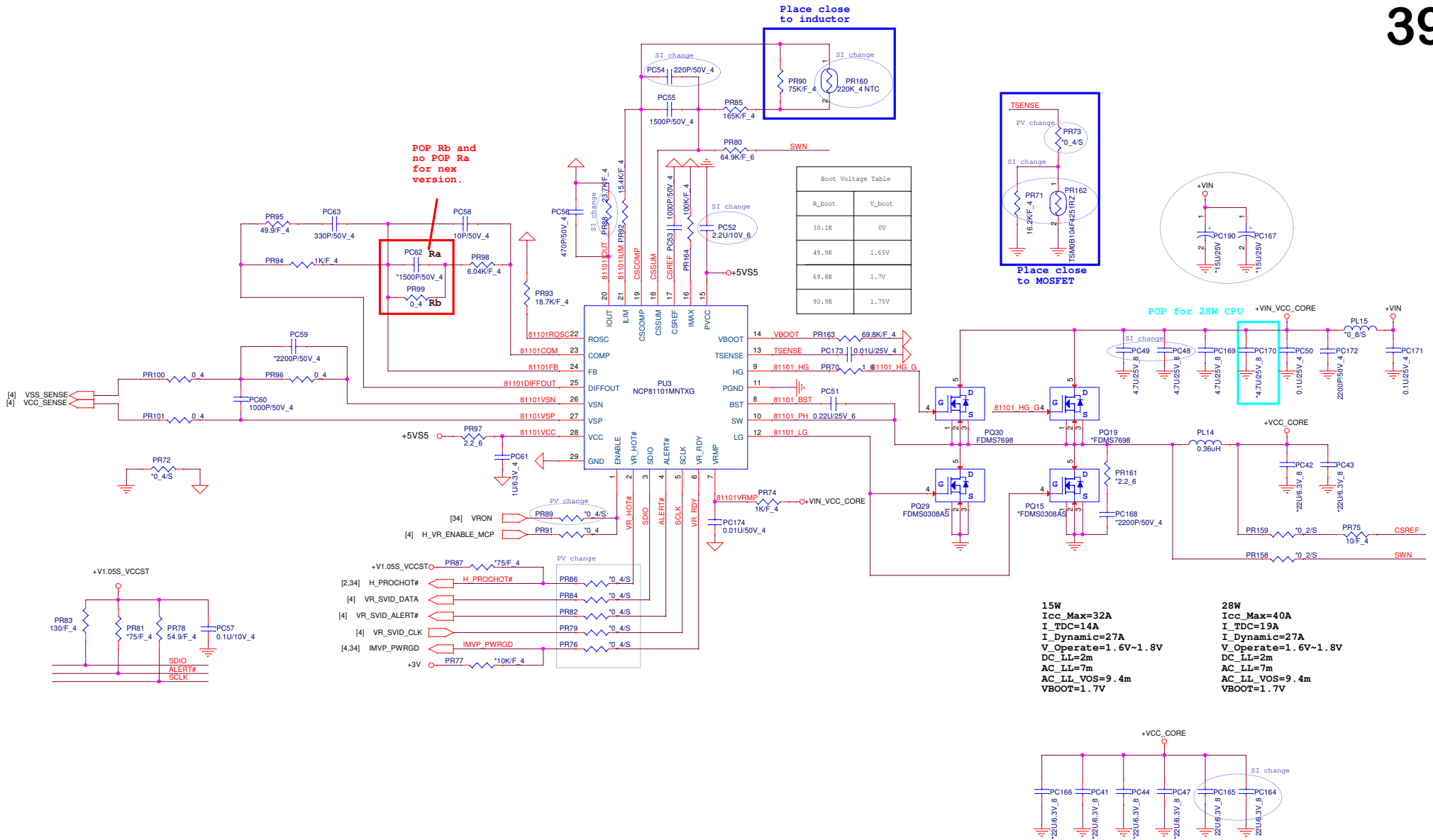
+VIN [24,26,29,30,35,36,37,39,40,41,42,43]
 +3VS5 [6,7,9,10,11,25,29,32,33,36,40,43]
 +5VS5 [13,25,29,32,36,37,39,40,41,42,43]



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Custom	+1.1VS5 (RT8228)/2.5V	1A
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NB5/RD3

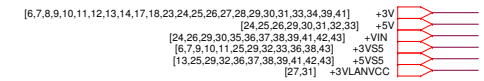
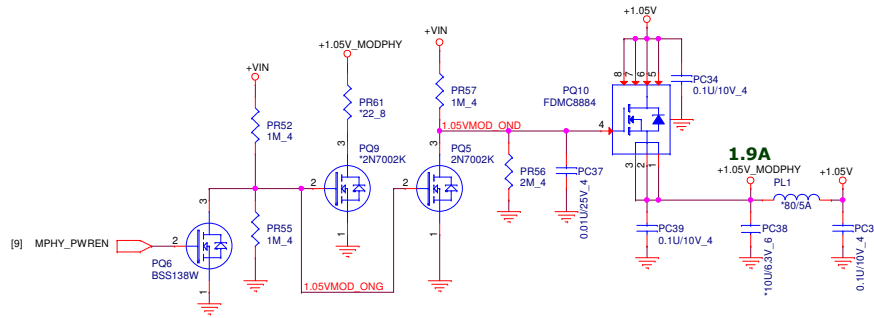
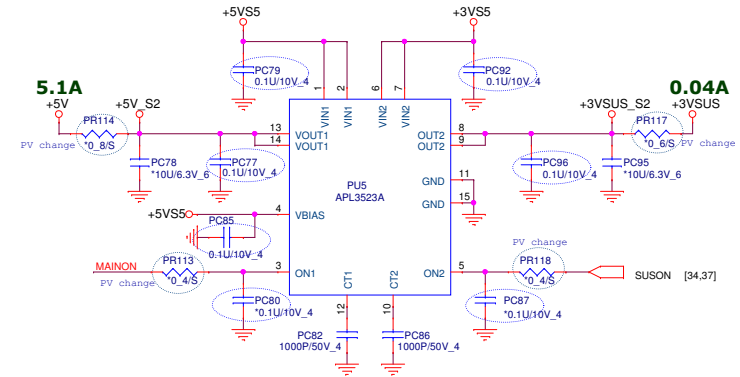
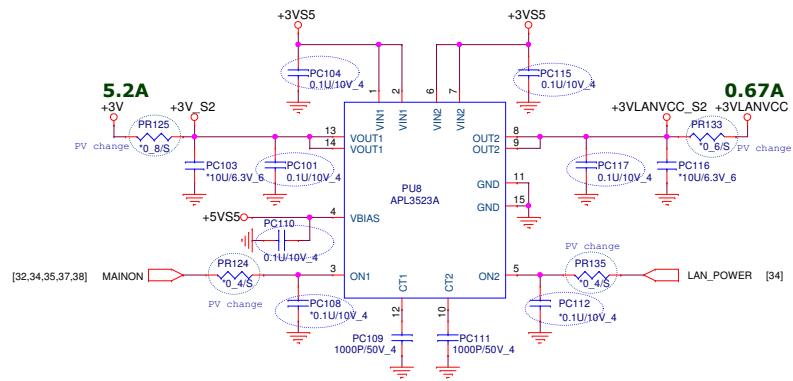


PROJECT :U83

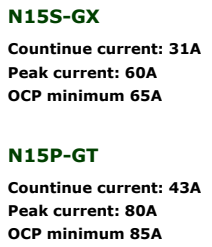
Quanta Computer Inc.

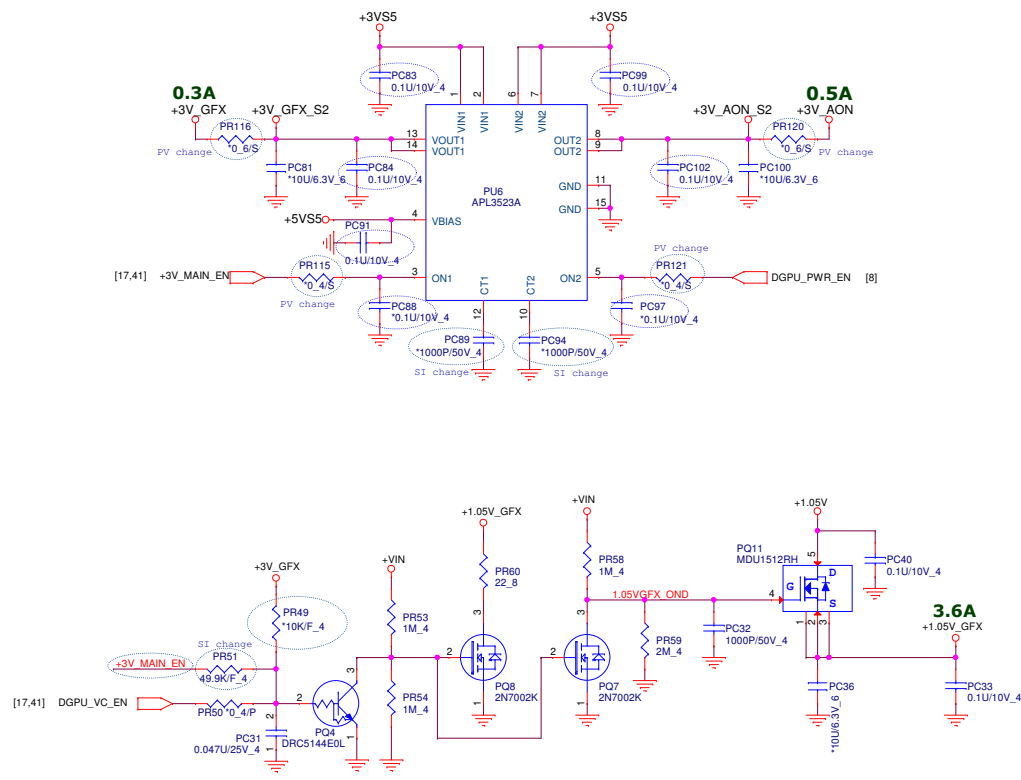
Size	Document Number	Rev
Custom	CPU Core (NCP81101)ULT	1A

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VGA TYPE	Ca, Cb
N15S-GX (25W)	No stuff
N15P-GT (35W)	Stuff





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Custom	1.05V_VGA/3V_VGA	1A
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Battery Connector	Pavillion	ENVY
14"	DFAD08MR063	DFAD08MR064
15"	DFAD08MR065	DFAD08MR066
17"	DFAD08MR063	DFAD08MR063

USB Charge Support	PR185	PR184
Pavillion	Stuff	NA
ENVY (USB charge)	NA	Stuff

UMA	Disable Page 41 、 42 、 43 ,but keep below location
Page 41	PC161 、 PC162
Page 42	PC138 、 PC144 、 PC4
Page 43	PC84 、 PC102 、 PC88 、 PC97 、 PC40 、 PC33

Discrete	Location	Part Number
N15S (25W)	PR155	CS29532FB10
	PC151 、 PC160	NA
	PQ21 、 PQ23 、 PQ25 、 PQ28	NA
N15P (35W)	PR155	CS31242FB13
	PC151 、 PC160	Stuff
	PQ21 、 PQ23 、 PQ25 、 PQ28	Stuff

Title		
<Title>		
Size A	Document Number <Doc>	Rev <Rev Co>
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